PROPOSED MODEL SPECIFICATION FOR UPDATED VSC-HVDC (VHVDC3)

TO: WECC MVS AND EPRI PROJECT P40A

FROM: PARAG MITRA, ELECTRIC POWER RESEARCH INSTITUTE (EPRI) INC.

SUBJECT: PROPOSED MODEL SPECIFICATION FOR UPDATED VSC-HVDC (VHVDC3)

DATE: MAY 2024

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The WECC model validation subcommittee (MVS) has been working on developing simple planning models for both powerflow and dynamic time-domain simulations in positive sequence software tools for HVDC point-to-point transmission. Models have been developed for both conventional line commutated converter (LCC) HVDC and voltage source converter (VSC) technology.

The powerflow models for conventional HVDC have always existed in the commercial tools. In the past roughly ten years, the MVS completed the definition of the VSC power-flow model, as well as work on several dynamic models. In 2017 one of the two simple LCC-HVDC dynamic models (*chvdc2*) was approved by WECC and has now been implemented and tested in the four major North American commercial tools (see [1]). In 2021, the first simple VSC-HVDC dynamic model (see [2]), the VHVDC1 model was approved by WECC. The VHVDC1 model is currently also being updated based on feedback from one independent VSC-HVDC owner/operator in WECC (see [3]). The updated model is expected to be named VHVDC2.

Similar to the VHVDC1 model, this memo proposes the specifications of a new VSC-HVDC model, the VHVDC3 model. The main differences of the VHVDC3 model from its predecessor (the VHVDC1/2) is as follows:

1. The VHVDC3 model has a voltage source interface like the REGC_B model instead of a current-controlled injection model at the grid interface (i.e., controlling the injected active and reactive power at every time-step) as with the VHVDC1 model.

2. The VHVDC3 model is capable of modeling VSC HVDC systems which implement grid forming controls at one end.

3. The VHVDC3 model can be used for modeling HVDC systems used for connecting offshore and remote renewable generation.

[1] https://www.wecc.org/Reliability/Memo_LCC_HVDC_Spec_070121.pdf and https://www.wecc.org/Reliability/Memo_022718.pdf

[2] https://www.wecc.org/Reliability/Memo_Spec_VSC-HVDC_102821_rev11.pdf

[3] https://www.wecc.org/Administrative/Pourbeik,%20P-%20MVS-%20Proposal%20to%20VHVDC1_September%202023.pdf

1.0 VHVDC3 dc line modeling:

The dc line model for the proposed VHVDC3 model is shown in Figure 1. This model, as with all the open and public models developed in MVS, is a generic model and does not represent exactly any equipment vendors HVDC system. The VHVDC3 can operate in:

1. Grid following mode on both ends, with one end regulating the dc bus voltage.

2. Grid forming mode on one end, and grid following mode on the other end. The grid following end will regulate the dc bus voltage.

Important: Note that *despite the representation* in Figure 1, the grid forming control can be implementable on either the rectifier end or the inverter end. Similarly, the grid following mode with dc bus voltage control can be implementable on either the rectifier or the inverter end. The depiction in Figure 1 only shows one of the possible configurations.

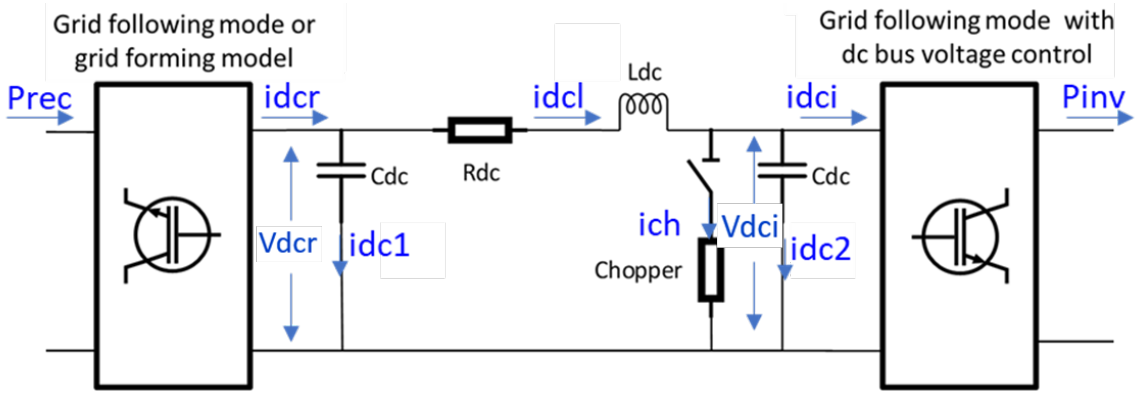


Figure 1 Dc line model for the proposed VHVDC3 model.

The power balance equation for the dc line is given by:

$$Prec * Eff_{rec} = Vdcr * Idcr\ , \tag{1}$$

$$Vdci * Idci * Eff_{inv} = Pinv, \tag{2}$$

where, Eff_{rec}, and Eff_{inv} are the rectifier and inverter efficiencies respectively, and all other quantities are as indicated in Figure 1. The equations for the dc voltages and the dc line current can then be written as:

$$Vdcr - Vdci = Idcl * Rdc - Ldc\frac{d(Idcl)}{dt} \tag{3}$$

$$Cdc\ \frac{d(Vdcr)}{dt} = Idcr - Idcl \tag{4}$$

$$Cdc\ \frac{d(Vdci)}{dt} = Idcl - Ich - Idci \tag{5}$$

$$Ich = \frac{Vdci}{Rch}, \text{when chopper is activated,} \qquad (6)$$

$$\text{else } Ich = 0$$

The chopper activation logic is given by:

$$\begin{aligned} &if\ Vdci > Vchopon, \text{chopper on,} \\ &if\ Vdci < Vchopoff, \text{chopper off} \end{aligned} \qquad (7)$$

where, *Vchopon* and *Vchopoff* are voltage thresholds for switching the chopper. These thresholds should be set by the user to have a hysteresis effect to prevent chattering of the chopper around the threshold value.

2.0 VHVDC3 grid forming control model:

The grid forming control structure is shown Figure 2. The model offers two types of grid-forming options: a) a droop based grid forming, and b) a virtual synchronous machine based grid forming structure[4]. The grid forming control in this model uses a two-level architecture, where the outer loop controls the voltage and the frequency/angle to generate the Id and Iq commands that are then enforced by a faster inner control loop. The dynamics of the inner control loop are represented by a time constant *Tg_r* [5].

The droop control in the model can be set by assigning an appropriate value for the parameter *Drp* in Figure 2, and setting the parameter *M* as 0. Note that when *M* is set to 0, the model automatically ignores the integrator. The virtual synchronous machine control can be activated by setting appropriate values for *d* (damping) and *M* (inertia constant) along with the desired *Drp* (droop). Note that for offshore wind applications, where a constant frequency control is desired on the offshore side, the value of *Drp* can be set 0 to prevent any frequency change due to change in active power.

The grid forming control also includes an outer loop frequency control, that brings the frequency back to the nominal value on the grid forming side when an addition or reduction of generation causes a deviation in the frequency. This outer loop is meant to be used for implementing isochronous control using the HVDC link for future applications.

3.0 VHVDC3 grid following control model:

The grid following active power control is shown in Figure 4. In the grid following mode, the converter end can either control the active power Figure 4(a) or the dc bus voltage Figure 4(b). In the active power control mode control, the converter follows the grid voltage phasor at the point of interconnection and injects *Id* corresponding to the active power reference. The active power controller includes an option to provide active frequency response (if it is possible during the operating conditions under study) using a deadband and droop, both of which can have different values for over and underfrequency conditions. **Frequency, for the primary frequency response controls, is**

[4] *Multilevel Modular Converter Average Model*, EPRI, Palo Alto, CA: 2022. 3002025736

[5] A, Yazdani, R, Iravani, *Voltage-Sourced Converters in Power Systems: Modeling, Control, and Applications*, Wiley IEEE press, March 2010

measured on the ac grid side of the converter. In the dc voltage control mode, the Id command is generated by a simple dc bus voltage controller. The dc bus voltage control ensures that the power injected into the link matches the power out of the link minus the dc line and converter losses.

The reactive power control loop for the grid following control is shown in Figure 3. This control is same as the VHVDC1 model and has the following options:

1. Voltage control with deadband (*dbd1*) and/or reactive droop (*Kc*), when *Refflag* = 1
2. Constant Q control with deadband (*dbd2*), when *Refflag* = 0
3. Constant power factor control with deadband (*dbd2*), when *Refflag* = 2

3.0 VHVDC3 voltage source interface:

Different from the VHVDC1 model, the proposed model uses a voltage source interface. As such the internal voltages *Ed* and *Eq* needs to be calculated for the network interface. While using the grid following control, the network interface is calculated as

$$Ed = Vt + Idcmd * Rfilt - Iqcmd * Xfilt, and \quad (8)$$

$$Eq = 0 + Iqcmd * Rfilt + Idcmd * Xfilt.$$

While using the grid forming control, the *Ed* and *Eq* are calculated as

$$Ed = Vd + Id * Rfilt - Iq * Xfilt, and \quad (9)$$

$$Eq = Vq + Iq * Rfilt + Id * Xfilt.$$

The *Ed* and *Eq* are then interfaced as a Thevenin voltage source shown in **Figure 5**. The time constant *Te* is included in the model for improving the numerical stability of the model.

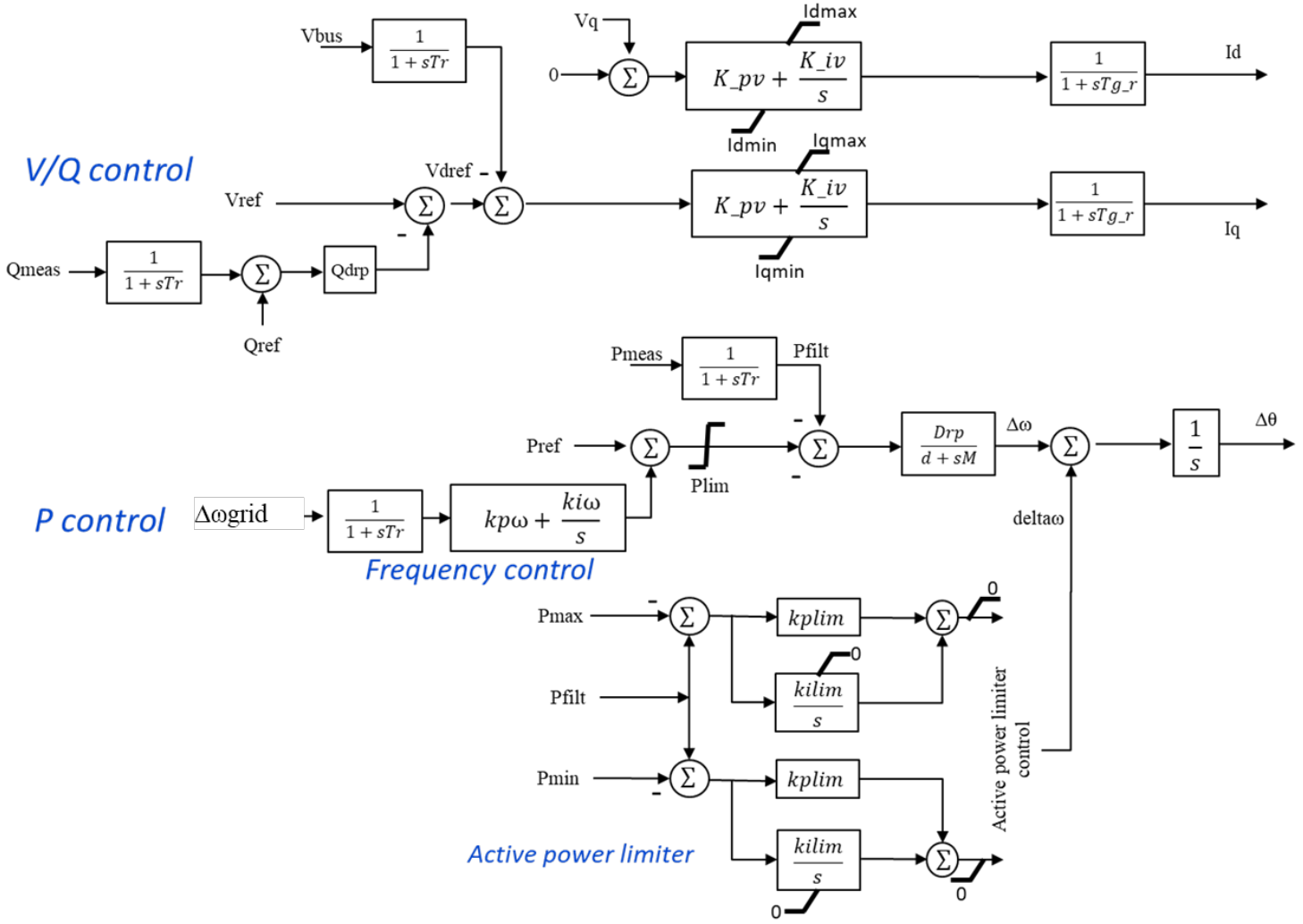


Figure 2 Grid forming control for the proposed VHVDC3 model.

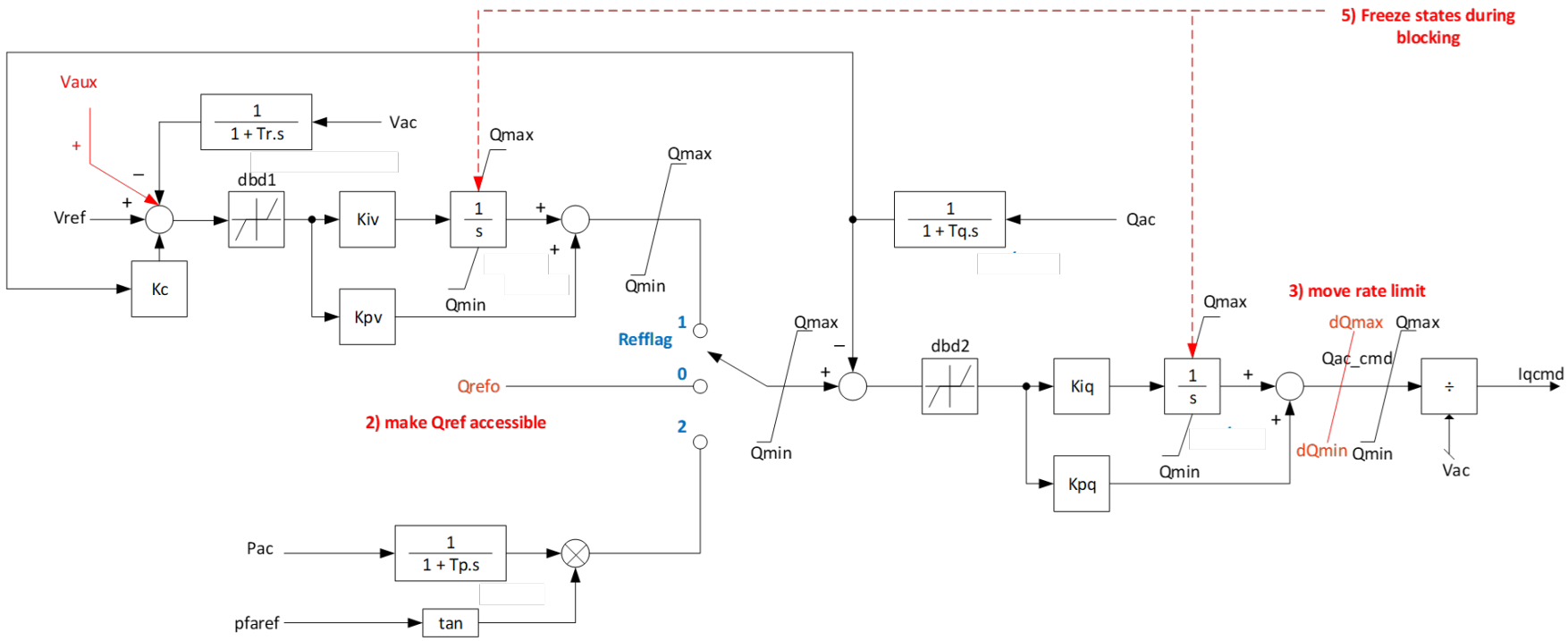
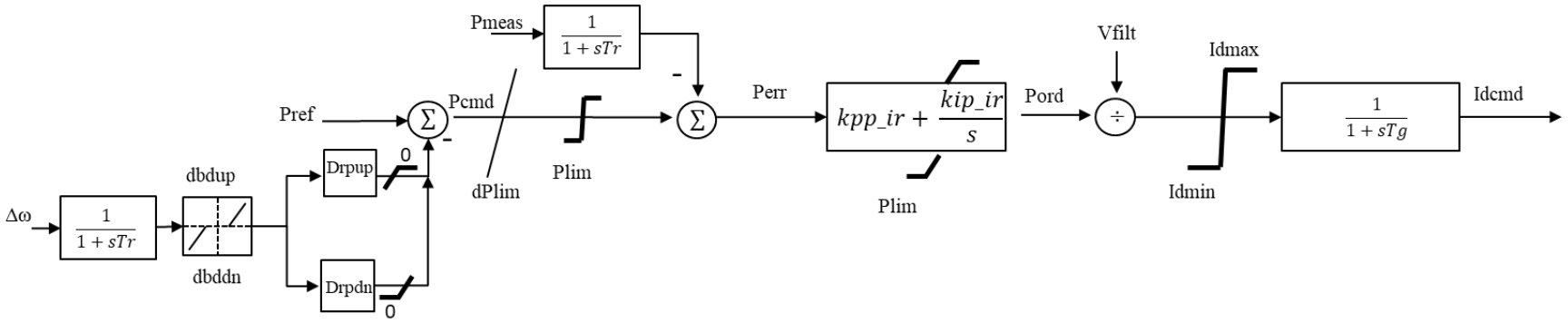
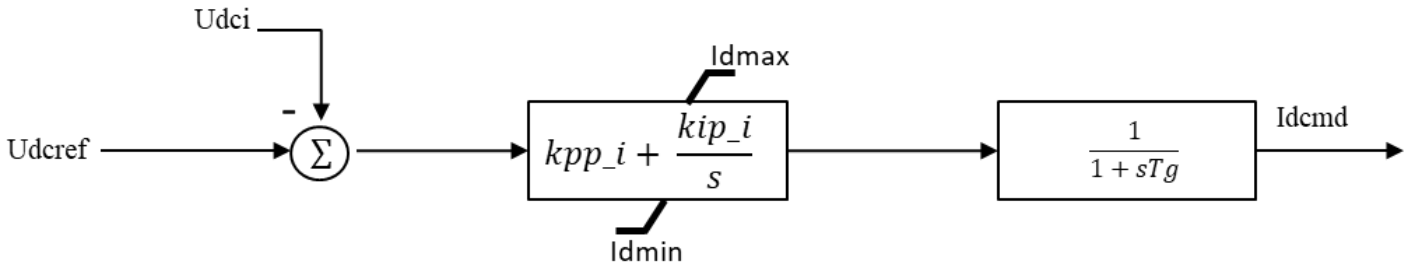


Figure 3 Grid following reactive power control for the proposed VHVDC3 model.



(a) Grid following active power control



(b) Grid following dc bus voltage control

Figure 4 Grid following active power control for the proposed VHVDC3 model.

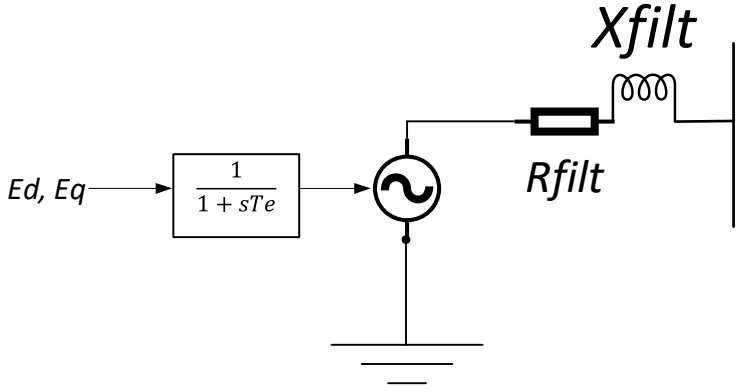


Figure 5 Network interface for the VSC HVdc model

5.0 Current limiter implementation:

The six (6) point piece-wise linear curve defined in Figure 6, allows an emulation of the reduction on the maximum allowable power reference (*Pmax*) as a function of the available ac voltage. That is, this function acts to dynamically change *Pmax* as shown in Figure 2. This is defined by the ten (10) parameters, *P1, P2, P3, P4, V1, V2, V3, V4, V5* and *V6*. This is same as that in the VHVDC1 model.

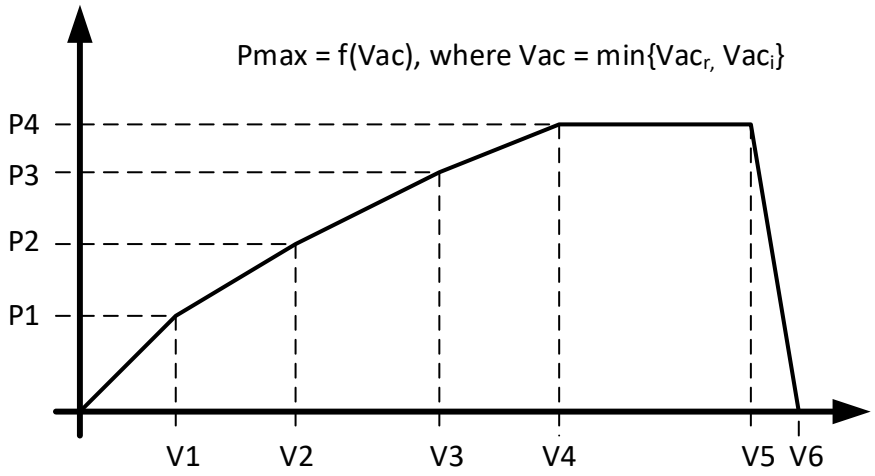


Figure 6 Power versus Voltage look-up table/curve for defining the maximum dc power reference as a function of ac voltage.

For implementing the current limit, the model implements two different options. Option 1 uses a D-curve implementation which is same as the VHVDC1 model. The D-curve is meant to be used at the converter end of the HVDC that operates in a grid following mode. Option 2 implements a total current magnitude limiter, which is meant to be used at the converter end that operates in a grid forming model.

Option 1: The current capability of the converters is modeled by a simple capability-curve as shown in **Figure 7**, and defined by the eight (8) parameters, *Imax, Idmax1, Idmax2, Idmax3, Idmax2, Idmax3, Idmin2* and *Idmin3*. Thus, independently, **on each** converter the current *Id* (active current being injected into the grid) is calculated at every time step and thus based on the current value of *Id, Iqmax/Iqmin* is determined from this capability-curve, and subsequently *Qmax/Qmin* is calculated as the value of *Iqmax* × *MWrating* and *Iqmin* × *MWrating*. Thus, real and reactive power are independently controlled on either side of the HVDC link, within the current ratings of the converter. Note that inherently the HVDC link is always in P-priority[6] – that is, real power always takes precedence.

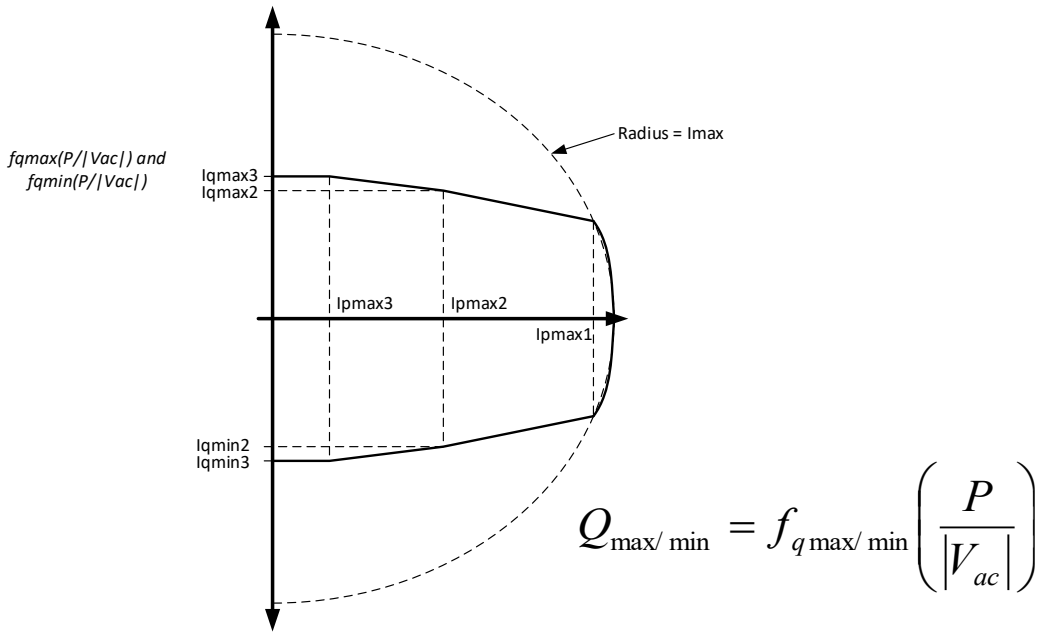


Figure 7: Definition of the reactive power capability of both converters (D-curve) as a function of dc power transferred and ac voltage.

Option 2: In this option the at current limit, the d and q axis currents saturated at their limits (Id_{lim} and Iq_{lim}) are calculated as:

$$if\ I > Imax$$

$$Id_{lim} = \frac{Id \times Imax}{\sqrt{Id^2 + Iq^2}}, and \qquad [10]$$

$$Iq_{lim} = \frac{Iq \times Imax}{\sqrt{Id^2 + Iq^2}}$$

[6] After initial discussion with vendors, there might be a need/desire to offer the possibility of Q-priority also in this simple model. This is to be further discussed in the future.

Note that option 2 is meant to be used with grid forming controls, where the action of the current limiter is to only limit the current magnitude without influencing the phase angle of the current command.

6.0 Protection Emulation:

Also included in the model is a simple representation of converter blocking for severe nearby ac faults. Each converter has its own blocking function, and the logic is as follows:

```
If Vac ≤ V_block
        Block = 1
Endif

If (Block = 1)
    If ( (Vac ≥ V_unblock) and Start_Unblock_Timer = 0) )
        Unblock_Timer = current_simulation_time
        Start_Unblock_Timer = 1
    Endif

    If ((Start_Unblock_Timer = 1) and (current_simulation_time – Unblock_Timer
≥ PLL_delay) )
        Unblock_Timer = 99999
        Start_Unblock_Timer = 0
        Block = 0
    Endif
Endif
```

The above is applied separately to both the rectifier and inverter side converters; thus, we have *Block_rec*, *Block_inv*, etc. Then the following logic is applied at the appropriate place in the code:

```
If (Block_rec = 1) or (Block_inv = 1)
    Pref = 0
    Idref = 0
Endif

If (Block_rec = 1)
    Qref= 0
    Iqref = 0
Endif

If (Block_inv = 1)
    Qref= 0
    Iqref = 0
Endif
```

In addition to blocking for ac system faults, the HVDC link also trips if the energy accumulated in the dc chopper exceeds a user defined threshold. The energy accumulation in the dc chopper circuit can be modeled as shown in **Figure 8**. Note that the dc chopper use and its protection is only applicable when the HVDC link is used to connect off-shore or remote renewables

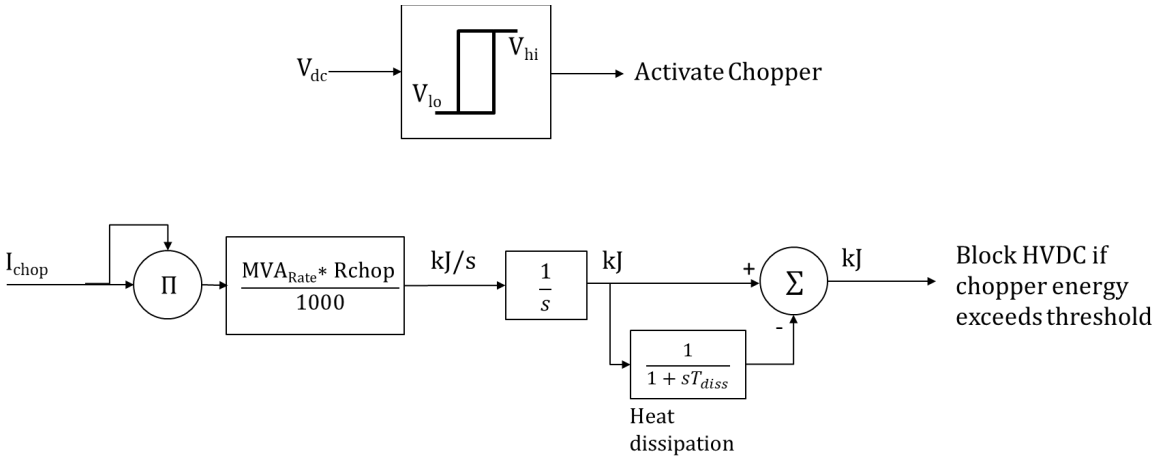


Figure 8: Dc chopper energy dissipation-based protection.

7.0 Important Notes

A few high-level statements about the control models presented in this specification are pertinent:

a. The model is not necessary representative of any vendor or equipment. The control loops are "general" and "simple" proportional-integral (PI) control loops, on the assumptions that PI control is a common control strategy.

b. The volt/var control loops (Figure 3) are intentionally quite similar to the high-level control-loop models in the *reec_a* model. This again is intentional, in order to give options of (i) voltage control with deadband/droop, or (ii) constant Q-control, or (iii) constant power-factor control.

Some of the salient points, and assumptions in proposing this model are as follows:

1. The intent of the model is for planning studies in positive-sequence programs such as GE PSLF™, Siemens PTI PSS®E, PowerWorld Simulator and PowerTech Labs TSAT™, and other similar tools. Thus, it should be understood that the model is not appropriate for studying the details of converter response and design to unbalanced disturbances.

2. Following on from point 1 above, this model is not intended, nor adequate, for studying the details of dc side faults. The dc-line (cable) dynamics model is rather rudimentary. Furthermore, positive sequence simulation platforms are likely not the best tool for studying dc-side phenomena.

Importantly for the dc-line dynamics, similar to the vhvdc1 and the chvdc2, ten (10) internal model integration steps should be performed to avoid numerical issues with the dc-line dynamics.