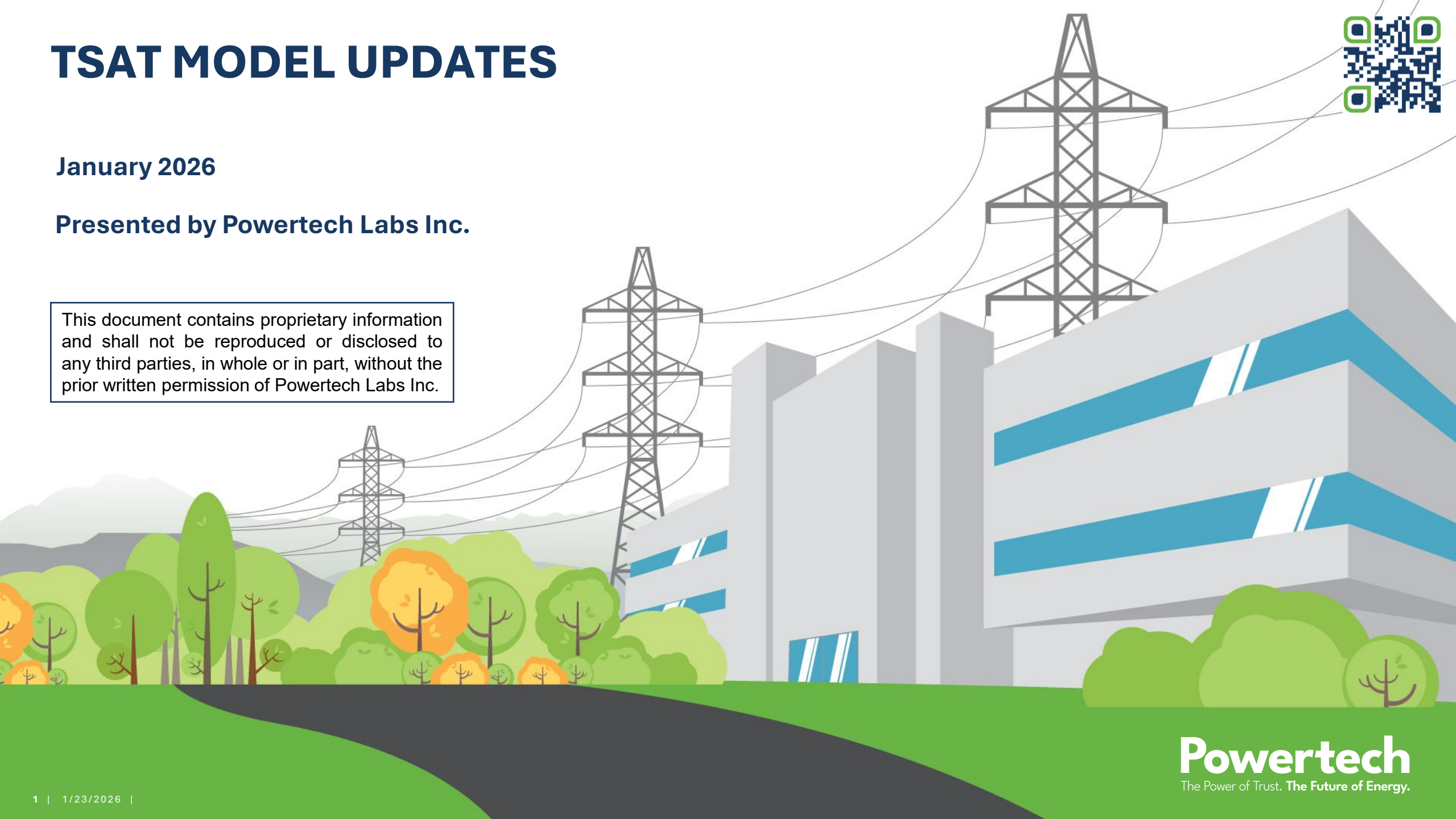
TSAT MODEL UPDATES

January 2026

Presented by Powertech Labs Inc.



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MODEL SUPPORT

• REGFM_A1 REGFM_B1	Supported since TSAT 25.1
• REGFM_C1 REPCGFM_C1	Template UDM available
• REEC_E REPC_D	Developed
• VHVDC2	Preliminary version supported

NEW MODEL FEATURES

- Centralized plant controller end block (PLT)
  - MVA-based scaling options
  - Voltage control initialization options
  - Monitor cumulative quantities among all downstream devices
- User-defined switching controls
  - New blocks in supervisory controllers to trip or insert components
- Regulation Path block (REG)
  - Added flexibility for back-calculation during initialization
- User-defined load model

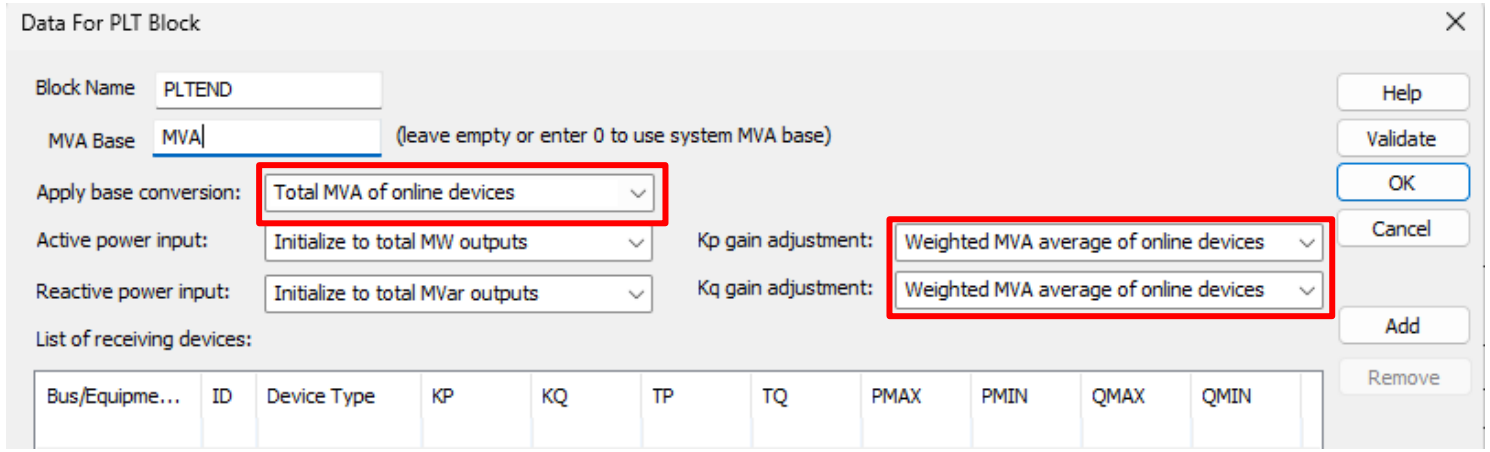
** SSAT Users – recommended to update to version 25.1.13+

Important updates for PLT block and supervisory controllers

CENTRALIZED PLANT CONTROLLER END BLOCK (PLT)

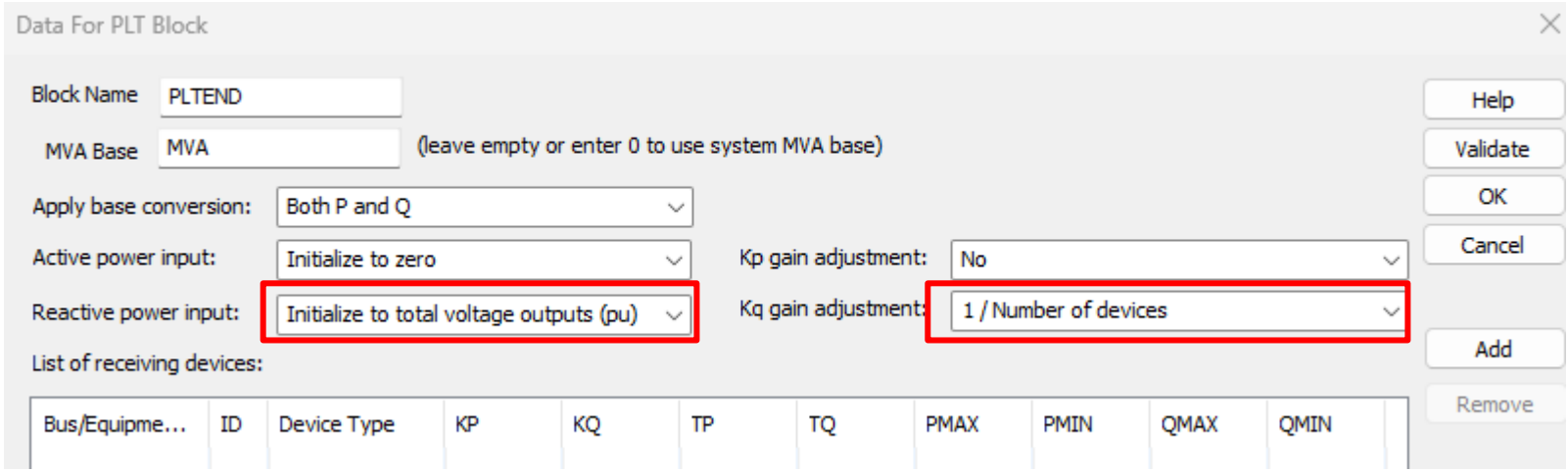
CENTRALIZED PLANT CONTROLLER END BLOCK (PLT)

- New device scaling options
  - Also used for REPC_D



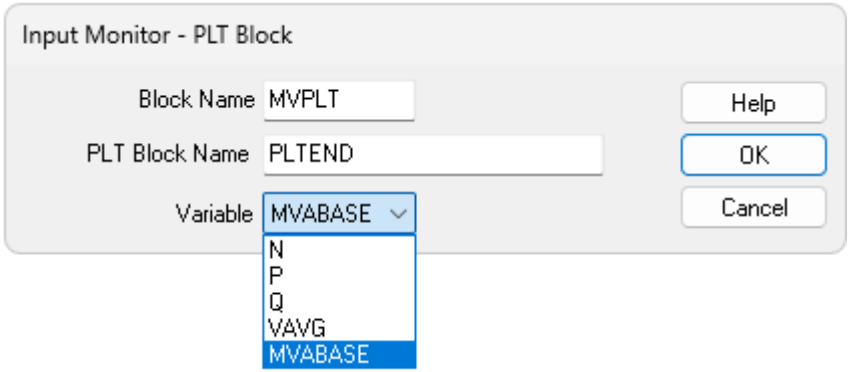
CENTRALIZED PLANT CONTROLLER END BLOCK (PLT)

- New initialization options for voltage control
  - Average voltage of online devices



MONITORING CENTRALIZED PLANT CONTROLLER END BLOCK (MON PLT)

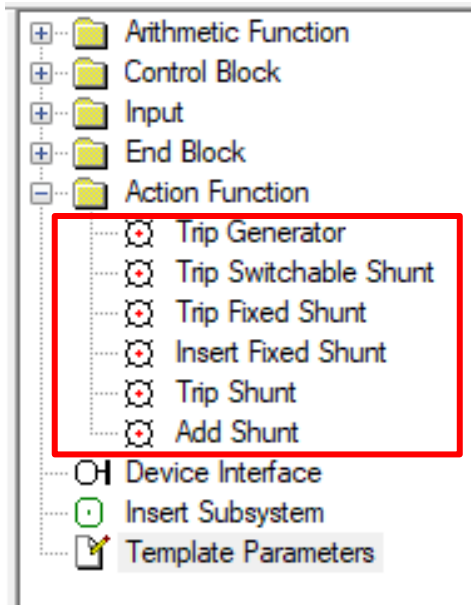
- New monitor block
- Returns summation of specified quantity of online devices listed in PLT block
  - Total number of online devices
  - Total MW, MVAr, MVA
  - Average voltage

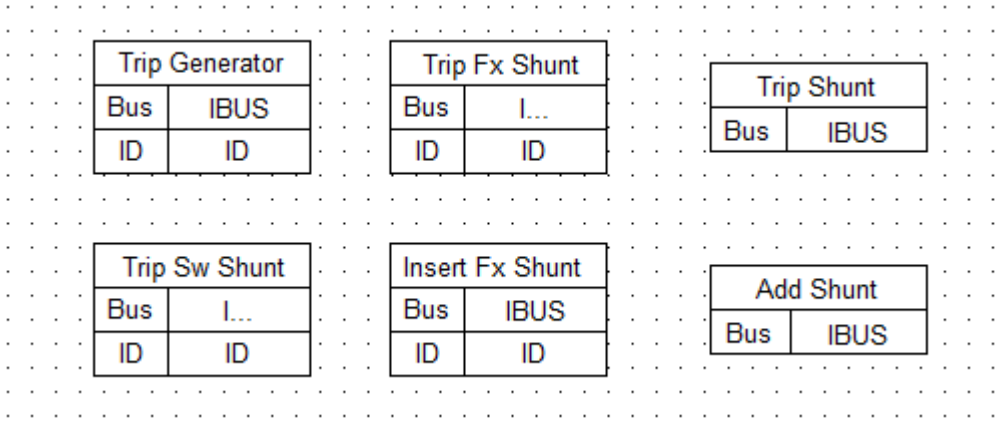


USER-DEFINED SWITCHING LOGIC

TRIPPING / INSERTING COMPONENTS

- New action blocks available in supervisory controllers
  - For implementing custom switching logic

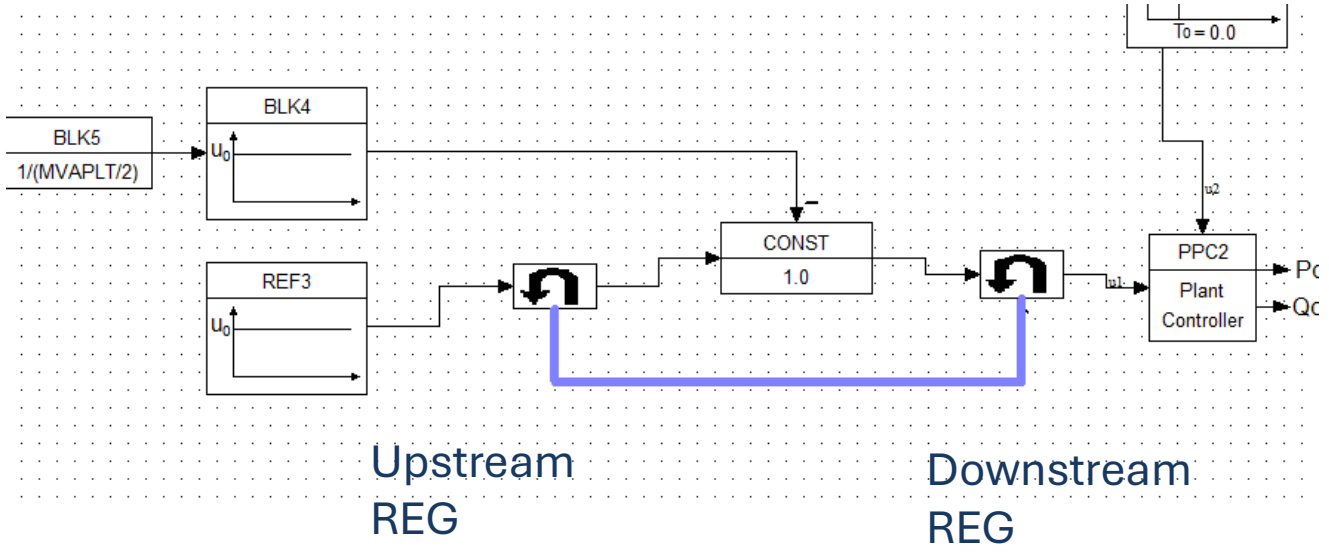




REGULATION PATH BLOCK

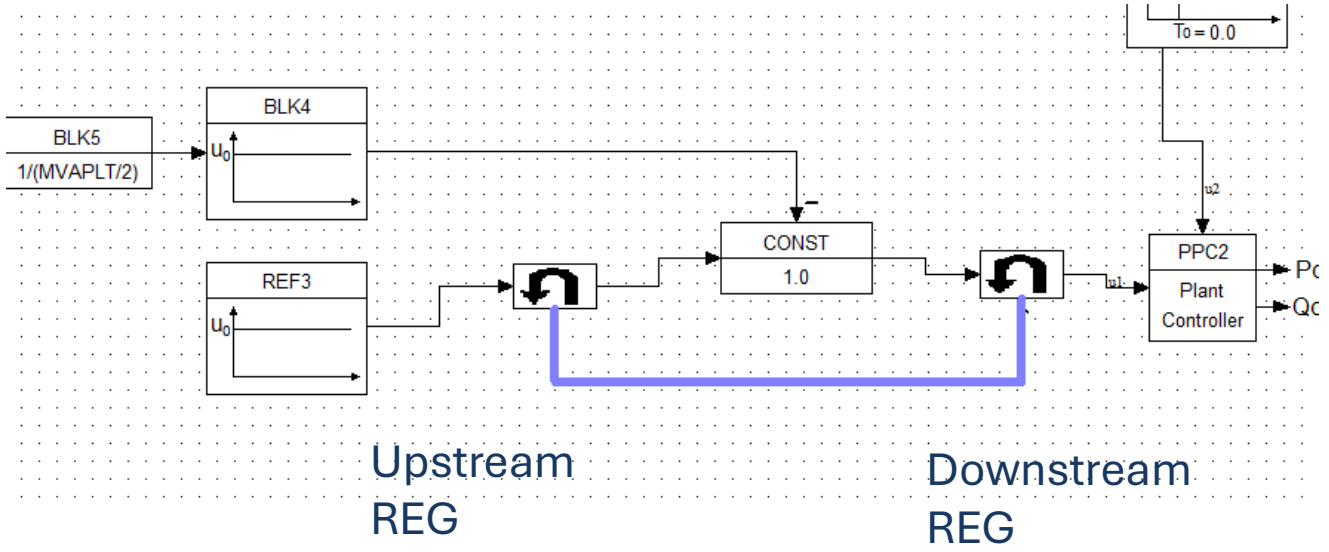
REGULATION PATH BLOCK

- The regulation path block causes back-calculation during initialization
  - Must not be on a REF path
  - Requires 2 blocks : upstream REG and downstream REG
  - User must connect these with a link in UDM Editor



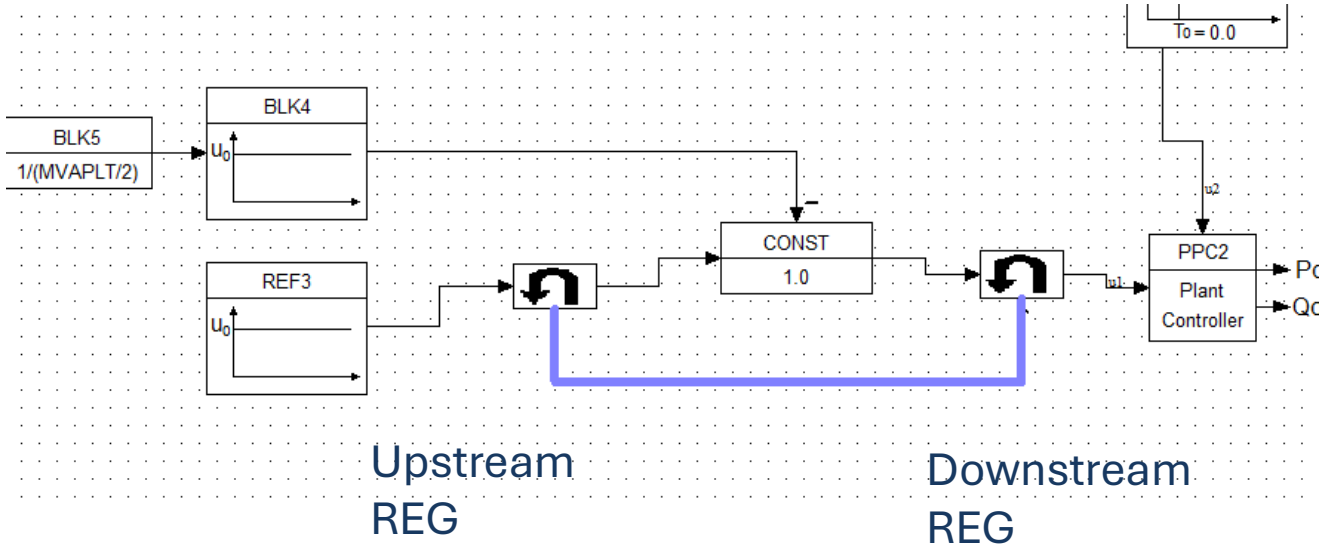
REGULATION PATH BLOCK

- Usage in hybrid supervisory controllers
  - REF and REF2 paths must connect to first PLT end block (as determined by XML file)
  - Use REG path blocks for 2nd , 3rd , and subsequent PLT end blocks. Time switch block may also work if you have already calculated correct output.



REGULATION PATH BLOCK

- Initialization process
  - Output of downstream REG is set to 0.
  - Output of upstream REG is calculated to achieve the downstream REG output. Block has an implicit summation. It adds an offset to other inputs to do this.



USER-DEFINED LOAD MODELLING

LOAD UDM IMPLEMENTATION

- Template WTGUDM as components in DSATools modular composite load model (CMPLD2)
- Will be moving to LDUDM format:
  - `Index, 'LDUDM', PFopt, PFval, template_name, template_parms`
  - Index : negative index to identify model in CMPLD2 records
  - Pfopt : option for assigning reactive power.
    - 1 = power factor specified in PFval, 0 = by fraction specified in PFval.
  - Pfval : power factor or fraction of MVAR load (between -1 and 1).
  - template_parms : these are the template parameters shown at the bottom of the Template Parameter Table window.

```
-10,'DISTEQ',  0 0.04 0.04 0
  0.08  1  1  1  0.9 1.1 0.00625
 1.025 1.04 30  5  0  0 /

-44 'LDUDM' 1.0 0.85 'PERC1'
 1 '1' -0.9 0.8 /


2  'CMPLD2' '1' 0,'', 0.0 0.0 0.0 0.0 -1.2
DISTEQ -10
LDUDM  -44  1.0 /
```

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