TO: WECC ATSM ADHOC GROUP

FROM: POUYAN POURBEIK, PEACE®; PPOURBEIK@PEACE-PLLC.COM

SUBJECT: PROPOSED CHANGES TO VHVDC1 FOR CREATING VHVDC2

DATE: 4/17/23 (REVISED 5/10/23; 8/23/24; 8/13/25)

CC: P. MITRA, EPRI

On 4/11/23 the group had a webcast/conference call to discuss the comments kindly shared by Raul Perez of NextEra Energy on 3/6/23, from their consultant Mitsubishi Electric Power Products, Inc. (MEPPI) Power Systems Engineering Division (PSED), on the vhvdc1 generic model. They (MEPPI) have compared the vhvdc1 model to a user-written model for the NextEra's Transbay Cable HVDC link. They thus came back with a number of recommendations.

For the call on 4/11/23, present were:

Samantha Deeney, MEPPI

Ning Lin, PowerTech Labs

Parag Mitra, EPRI

Saurav Mohapatra, PowerWorld

Raul Perez, NextEra Energy

Pouyan Pourbeik, PEACE®

Shruit Rao, GE

David Roop, MEPPI

Juan Sanchez-Gasca, GE

Jay Senthil, Siemens PTI

Chris Stauffer, MEPPI

Doug Tucker, WECC

Song Wang, Portland General Electric (WECC MVS Chair)

Jamie Weber, PowerWorld

This revision 4 of the specifications for vhvdc2 incorporates slight modifications to the original memo based on decisions made during a group virtual meeting on 8/13/25 at 1 pm US Central Time. Attendees at that call were: Wei Du, PNNL; Ning Lin, PowerTech Labs; Parag Mitra, EPRI; Raul Perez, NextEra Energy; Pouyan Pourbeik, PEACE®; Quan Nguyen, PNNL; Jay Senthil, Siemens PTI, Ramin Vakili, GE Vernova; Song Wang, PGE; and Jamie Weber, PowerWorld

The comments from MEPPI were discussed at length by the group, and based on mutual consultation among all parties the following conclusions and decisions were made:

1. There were a total of nine (9) recommendations made by MEPPI [1] – see a very brief summary in the Appendix below. The details are in [1].
2. The group agreed that:

a. Recommendation 9 would not be implemented in a new version of the *vhvd*c model, since it appears to be very vendor specific. Furthermore, all agreed that the current generic models implementation of applying the "emulated" PLL delay from after fault clearing probably makes more sense in general since in actual equipment the voltage would need to first recover before an attempt is made to un-block.

b. The issues described in recommendations 7 and 8 would most likely be alleviated much by simply addressing recommendations 3, 4, 5 and 6.

c. Thus, the group agreed to work on recommendations 1, 2, 3, 4, 5 and 6. A new model would thus be developed, called *vhvdc2*.

3. Below the decisions made on how to address recommendation 1 through 6 are detailed.

Recommendation 1 – The key recommendation here was to allow for a remote bus in the power flow to be the point of measurement and control for each of the two converter stations. Thus, the decision was to introduce six (6) more parameters in the dynamic model, as follows:

FBUSI – from bus for defined branch on inverter side

TBUSI – to bus for defined branch on inverter side

IDI – branch ID

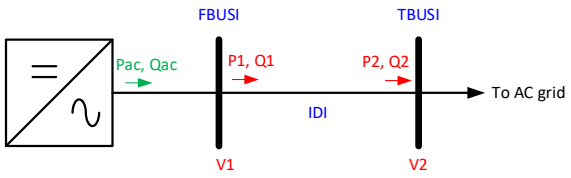
FBUSR – from bus for defined branch on rectifier side

TBUSR – to bus for defined branch on rectifier side

IDR – branch ID

The approach would be identical on both sides. Figure 1 below helps to explain the approach on the inverter side, with the rectifier side being the same.

As shown in Figure 1, one of two approaches can be taken. One to implicitly include the converter transformer in the loss calculations in the converter power flow model. Secondly, to explicitly model the converter transformer in power flow. It is extremely important to note that either way, the path from the converter to the most remote bus (TBUSI) must be completely radial. **Important Note:** A simple way that this can be checked in each software tool is that if P1 (or P2) < 0.95×Pac then a waring message should be given to the user "*WARNING! Measured AC Power is significantly less than AC power coming out of the converter at bus XX, ensure that defined branch is radial to converter!*". Also, if the defined branch is ill-defined (i.e., a nonexistent branch) then Pac, Qac and V ac at the POI of the converter is used, and a warning message given to the user to this effect.



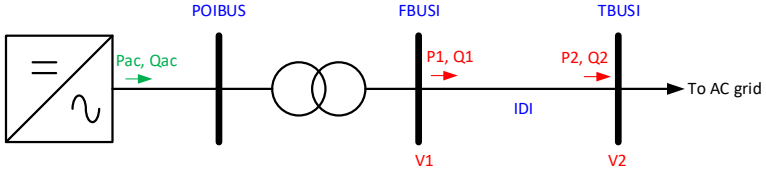


Figure 1: Proposed changes to include a remote bus point of measurement and control.

Above said, the following should be done assuming the defined branch is correct and radial:

- P and Q are always calculated in the direction of FBUSI → TBUSI
- P1, Q1 and V1 are the measured values used in the model for P, Q and V ac control if TBUSI is a positive number
- P2, Q2 and V2 are the measured values used in the model for P, Q and V ac control if TBUSI is a negative number. (Note: the idea here is that when TBUSI is entered as a negative number, then clearly |TBUSI| is what is used in monitoring the branch, but the -ve sign indicates that the measurements are to be made on the TO end of the branch. Alternatively, an extra model parameter could be defined to indicate whether the FROM or TO end measurement points are to be used).

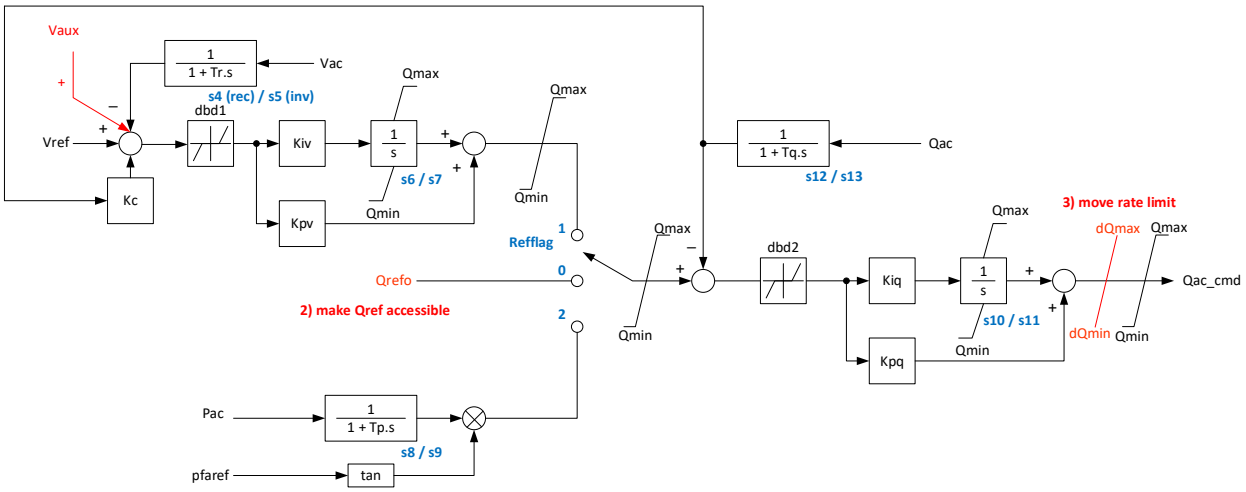
Recommendation 2 – Add user access to ***Qrefo*** (see Figure 2 below). As an aside two other items were also discussed. First, to also add ***Vaux*** as an additional input accessible by the user. Secondly, to add another parameter to the dynamic model:

MVAbase AC – if it is set to zero then ***MWrate*** is used for this value. If both this parameter and MWrate are set to zero, then an ERROR message is given to the user upon initialization and the simulation stops requesting the user to fix this.

Thus, ***MWrate*** (which is an existing parameter in vhvdc1) is used as the per unit base of all MW quantities, i.e., ***Pmax***, ***Pmin***, ***dPmax***, ***dPmin***, ***Pref***, ***p1***, ***p2***, ***p3***, and ***p4***.

Thus, ***MVAbase AC*** is used as the per unit base of all MVar quantities and maximum ac current limit, i.e., ***Imax***, ***Kcr***, ***Kci***, ***dbd2r***, ***dbd2i***, ***Kpvr***, ***Kivr***, ***Kpqr***, ***Kiqr***, ***Kpvi***, ***Kivi***, ***Kpqi***, ***Kiqi***, ***dQmax***, ***dQmin***, ***Qref_i***, ***Qref_r***, ***Ipmax1***, ***Ipmax2***, ***Ipmax3***, ***Ipmin1***, ***Ipmin2***, ***Ipmin3***, ***Iqmax2***, ***Iqmax3***, ***Iqmin2*** and ***Iqmin3***.

Recommendation 3 – Move the ramp rate in the Q/V controls to the new location show in Figure 2 below. The software vendors indicated that they would implement this ramp rate as a numerically solved rated rate, rather than introducing a new state in the model with a very small time-constant.



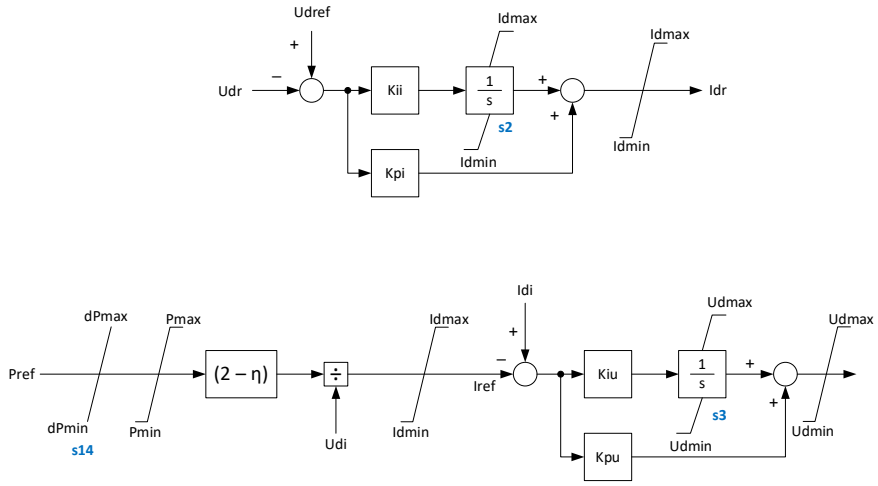


Figure 2: Proposed changes to the controller parts of the *vhvdc1* model.

Recommendation 4 – Add new parameters to define a look-up table for changing the blocking voltage at the inverter/rectifier as a function of active power (MW) being transferred by the HVDC link (see Figure 3).

Thus, vblk_inv and vblk_rec are removed as user input parameters from the dynamic model, and instead we introduce the following parameters, i.e.

pbr1 – power (pu on MWrate) point 1 on rectifier side

pbr2 – power (pu on MWrate) point 2 on rectifier side

pbr3 – power (pu on MWrate) point 3 on rectifier side

pbr4 – power (pu on MWrate) point 4 on rectifier side

vbi1 and ***vbr1*** – ac voltage (pu) point 1 on inverter/rectifier side

vbi2 and ***vbr2*** – ac voltage (pu) point 2 on inverter/rectifier side

vbi3 and ***vbr3*** – ac voltage (pu) point 3 on inverter/rectifier side

vbi4 and ***vbr4*** – ac voltage (pu) point 4 on inverter/rectifier side

The two sets are independent in the voltage set points.

Important Notes:

- The power points must be monotonic, i.e., $1 \geq pbr4 > pbr3 > pbr2 > pbr1 \geq 0$
- If $pbr4 < 1$, then $vblk\_* = vb*4$ for all power levels above ***pbr4***
- If $pbr1 > 0$, then $vblk\_* = vb*1$ for all power levels below ***pbr1***, down to 0 pu power
- The above three relationships apply to the both the inverter and rectifier side parameters.
- The voltage here refers to the voltage at the AC bus which is the point of measurement (POM) for the converter. That is, each converter side will block independently when the filtered Vac at the POM (e.g., voltage at V1 or V2, see recommendation 1) falls below the *vblk* coming out of this function.
- The value of P used on the x-axis of the four (4) point piecewise linear curves is the initial DC power transfer across the HVDC link upon model initialization on the rectifier side.

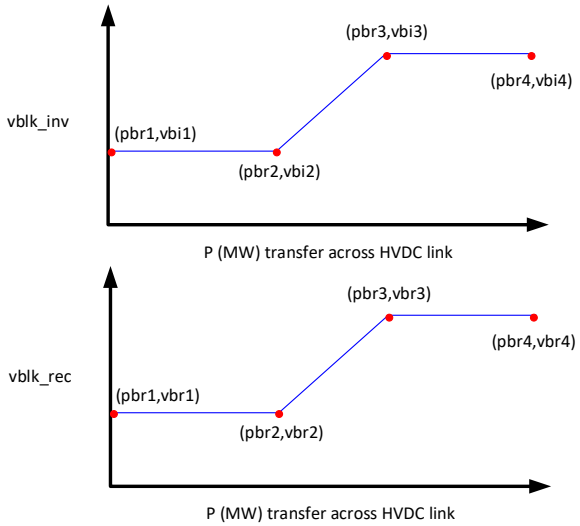


Figure 3: Proposed V vs P lookup curve for determining the blocking voltage at the inverter/rectifier end as a function of active power (MW) transfer.

Recommendation 6 – during the network solution iterations, at the interface of the dynamic converter models and the network solution, it would be best to try to impose a limit on the total AC current injected into the grid. Namely, to limit the total injected current to a maximum of ***Imax*** pu on ***MVAbase AC***.

References:

Chris Stauffer, Samantha Deeney and David Roop, MEPPI, *PSLF Generic Model Limitations*, February 23, 2023

Appendix: MEPPI Model Recommendations

1. Make changes to the VSC power flow model in the software tools to allow for explicitly modeling the HVDC converter transformer, rather than implicitly including in the loss factors.
2. Add user access to Qrefo (see Figure 1 below)
3. Move the ramp rate in the Q/V controls (see Figure 1 below)
4. Add new parameters to define a look-up table for changing the blocking voltage at the inverter/rectifier as a function of active power (MW) being transferred by the HVDC link (see e.g. Figure 2)
5. Freeze all controller states of the model during inverter/rectifier blocking (see Figure 1 below) – it was decided on the 8/13/25 call to not implement this recommendation for now.
6. Limit the current injection at the converter interface to the Imax of the converter during faults – this requires getting inside the network solution algebraic equations.
7. Initial reactive power influences fault response characteristic and magnitude for the user model, but not for the generic.
8. Generic model reactive power limits are open to align fault response more closely with the TBC user model.
9. Add an option/flag to the model to allow the user to select whether the Tdelay imposed for inverter/rectifier blocking applies starting from: (i) fault inception, or (ii) after fault clearing and when the voltage recovers above the blocking voltage. Presently, the model applies the delays in only the latter way.