TESTING THE CHVDC2 MODEL

TO: WECC HVDC TF

FROM: POUYAN POURBEIK, PEACE

SUBJECT: PROPOSAL FOR TESTING THE CHVDC2 MODEL

DATE: AUGUST 23, 2017 (REVISED 9/11/17; 9/28/17; 10/3/17; 02/27/18)

CC: ANISH GAIKWAD, EPRI

In [1] two proposed generic models for a line-commutated converter (LCC) HVDC were presented. These were tentatively approved by the WECC HVDC TF and at subsequent meetings of the WECC HVDC TF and MVWG it was decided that the *chvdc2* model would be pursued as the initial implementation of a standard LCC HVDC model across the main commercial software tools.

Presently, the four commercial software vendors GE PSLF, Siemens PTI PSS®E, PowerWorld Simulator and PowerTech Labs TSAT™, have adopted the *chvdc2* model. The model is also now WECC approved. This simple test plan was developed to provide a means of benchmarking and testing the model across the four software platforms.

As of 2/27/18 all four software vendors have finalized the model and run these tests, and graciously provided their respective results to be plotted together here. Appendix D shows the comparison of the simulation results across all the four platforms for all the test cases. As can be seen there is good match across all the tools (and all these results are also consistent with the original user-written models [1]). We are of course tremendously indebted to all the four commercial tool vendors for their efforts in this work.

1.0 Test Case:

A simple benchmark test case system, based on the CIGRE benchmark case [2], was established for testing the model. The data for the model is provided below.

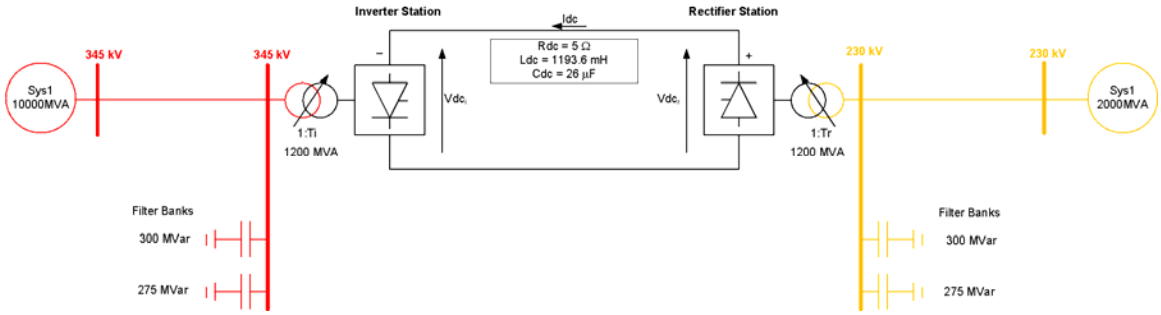


Figure 1: Simple CIGRE benchmark case.

Main Circuit Data

R = 5 Ω, L = 1193 mH, C = 26 µF
V = 500 Vdc, I = 2000 A

Each converter has 2 bridges

Parameter	Rec	Inv
Vdiode (per bridge) kV	0.01	0.01
Xcomm (per bridge) Ohms	6.7	6.7
Rtran (per bridge)	0.0036	0.0036
Xtran (per bridge)	0.18	0.18
Vbase AC kV	230	345
Vbase DC kV	211	211
Xfmr MVA	1200	1200
Fxd AC Tap	1	1
Fxd DC Tap	1	1
Adj AC Tap	1.05	1.07
Adj DC Tap	1	1
tap min	0.95	0.93
tap max	1.05	1.07
tap step	0.01	0.01
Max V	0.9	0.9
Min V	1.1	1.1
Xsmooth (mH)	100	100

Power Flow and Dynamics Data:

The power flow solution is shown in Figure 2 and Table 1. The dynamic model parameters are given in Appendix A. The two classical generators at Bus 1 and 4 are identical and modeled using *gencls*, with the following parameters: MVA = 10000, H = 999999, D= 0, Ra = 0 and X"d = 0.18

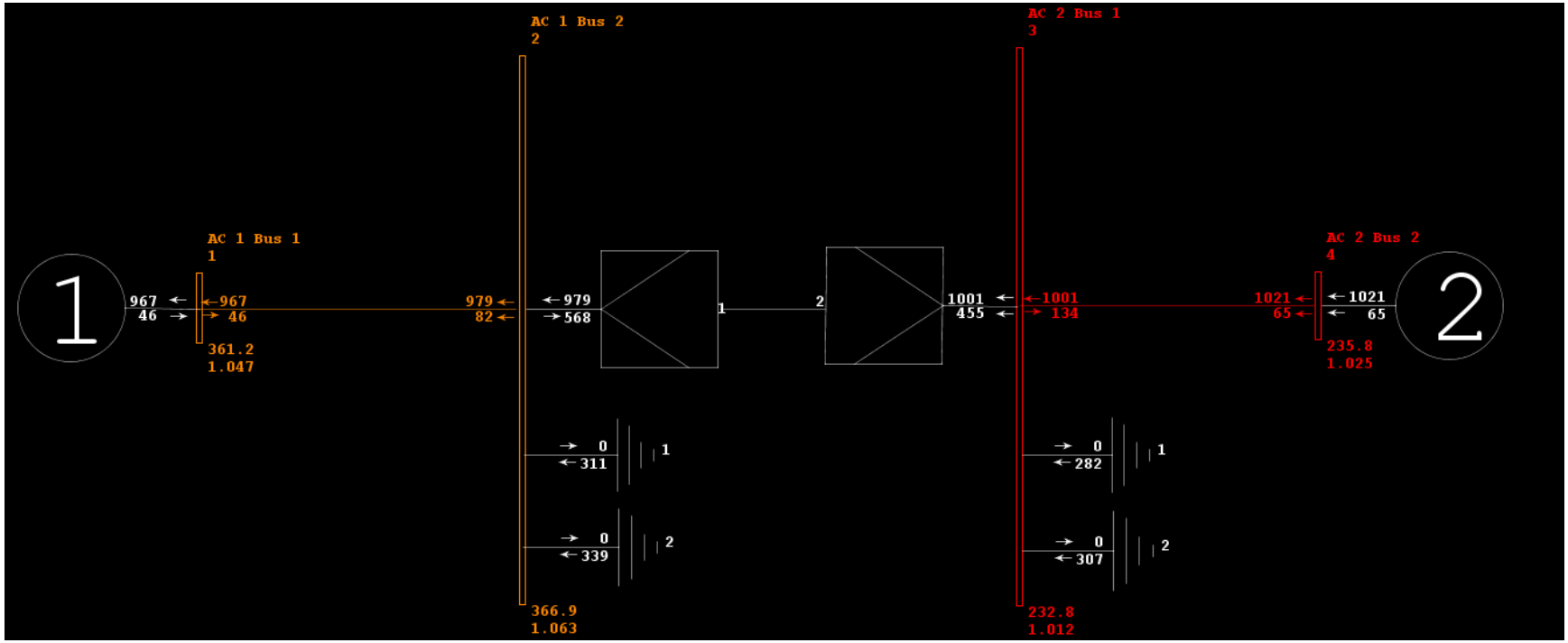


Figure 2: Test case power flow solution.

Table 1: Power Flow solution

BUS-NO	NAME	KV	TP	VSCHED	V-PU	DEG
1	AC 1 Bus 1	345	0	1.047	1.047	-3.98
2	AC 1 Bus 2	345	1	1.048	1.0634	3.54
3	AC 2 Bus 1	230	1	1	1.012	-11.28
4	AC 2 Bus 2	230	0	1.025	1.025	0

BUS-NO	NAME	KV	ID	ST	P	Q
1	AC 1 Bus 1	345	1	1	-966.5	46.1
4	AC 2 Bus 2	230	2	1	1020.6	64.8

BUS-NO	NAME	KV	CNV BUS	NAME	KV	ID	ST	TYPE	PSCHED	IDC SCHD	VDC SCHED	PAC	QAC	IDC	VDC	ALPHA	GAMMA	ALPH MIN	GAMMA MIN
3	AC 2 Bus 1	230	17	DC Rec	422	2	1	REC	1000	2000	500	1000.7	454.6	2000	500	16.87	15	5	15
2	AC 1 Bus 2	345	18	DC Inv	422	1	1	INV	0	2000	500	-979.3	568.2	2000	490	15	24.45	110	18

2.0 Test Simulations:

The following two simulations should be performed:

1. Test 1: (integration time step = 0.0005 sec)
    a. Run for one second with no-disturbance
    b. Place a fault at bus 1 (inverter side)
    c. Fault impedance X = 0.005 pu
    d. Remove fault at 1.05 seconds (i.e. 50 ms fault duration)
    e. Run to 5 seconds
2. Test 2: (integration time step = 0.0005 sec)
    a. Run for one second with no-disturbance
    b. Place a fault at bus 4 (rectifier side)
    c. Fault impedance X = 0.005 pu
    d. Remove fault at 1.05 seconds (i.e. 50 ms fault duration)
    e. Run to 5 seconds
3. Test 3
    a. Play the waveforms for voltage (frequency is constant) shown in Figure 3 in as a source at bus 1 (inverter side) and bus 4 (rectifier side), respectively.
    b. The frequency is constant at 60 Hz on both sides
    c. The voltage on the rectifier side (bus 4) is constant at its initial value of 1.025 pu
    d. The voltage on the inverter side (bus 1) is constant at 1.047 pu from 0 to 1.0005 seconds; falls to 0.8 pu from 1.0005 seconds to 1.05 seconds; and is again constant at 1.047 pu from 1.0505 seconds to 2 seconds.
    e. The waveforms (and the simulation) are sampled at 0.0005 second intervals.
4. Test 4
    a. Play the waveforms for voltage (frequency is constant) shown in Figure 4 in as a source at bus 1 (inverter side) and bus 4 (rectifier side), respectively.
    b. The frequency is constant at 60 Hz on both sides
    c. The voltage on the inverter side (bus 1) is constant at its initial value of 1.047 pu
    d. The voltage on the rectifier side (bus 4) is constant at 1.025 pu from 0 to 1.0005 seconds; falls to 0.8 pu from 1.0005 seconds to 1.05 seconds; and is again constant at 1.025 pu from 1.0505 seconds to 2 seconds.
    e. The waveforms (and the simulation) are sampled at 0.0005 second intervals.

VERY IMPORTANT NOTE: Although, as is clear from the simulation results since gamma goes to zero, in the case of the inverter fault more than likely there would be commutation failure, for this simulation we deliberately choose NOT to emulate commutation failure (by shorting invoking inverter bypass). This is to keep the comparison of the tests as simple as possible.

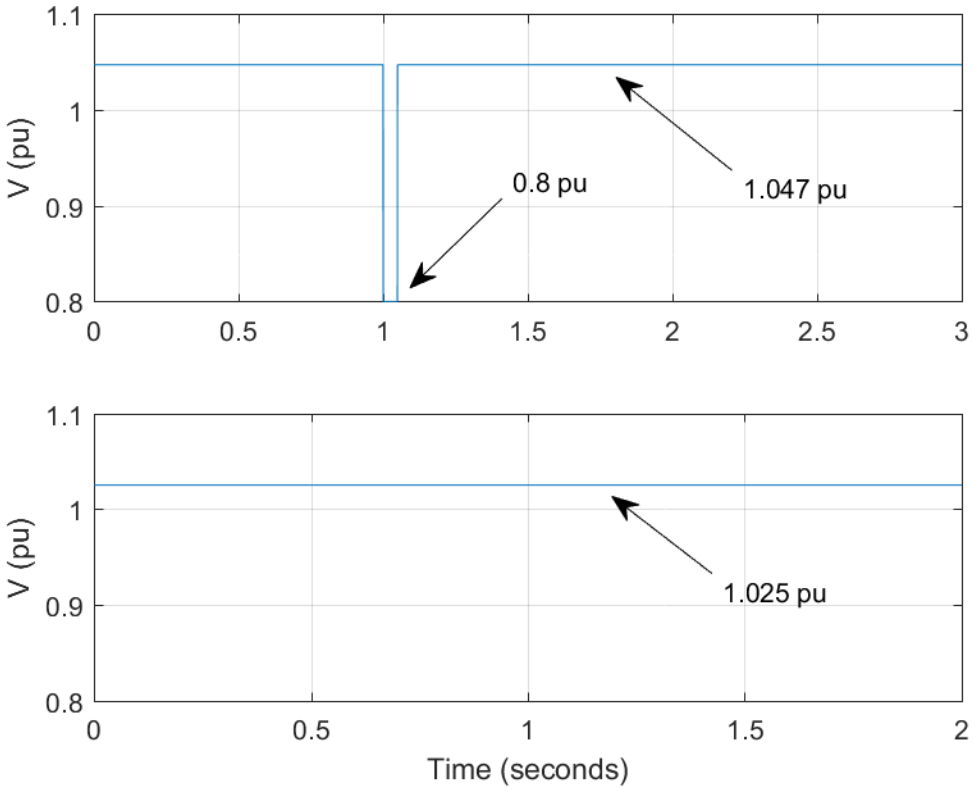


Figure 3: Voltage waveforms for Test 3.

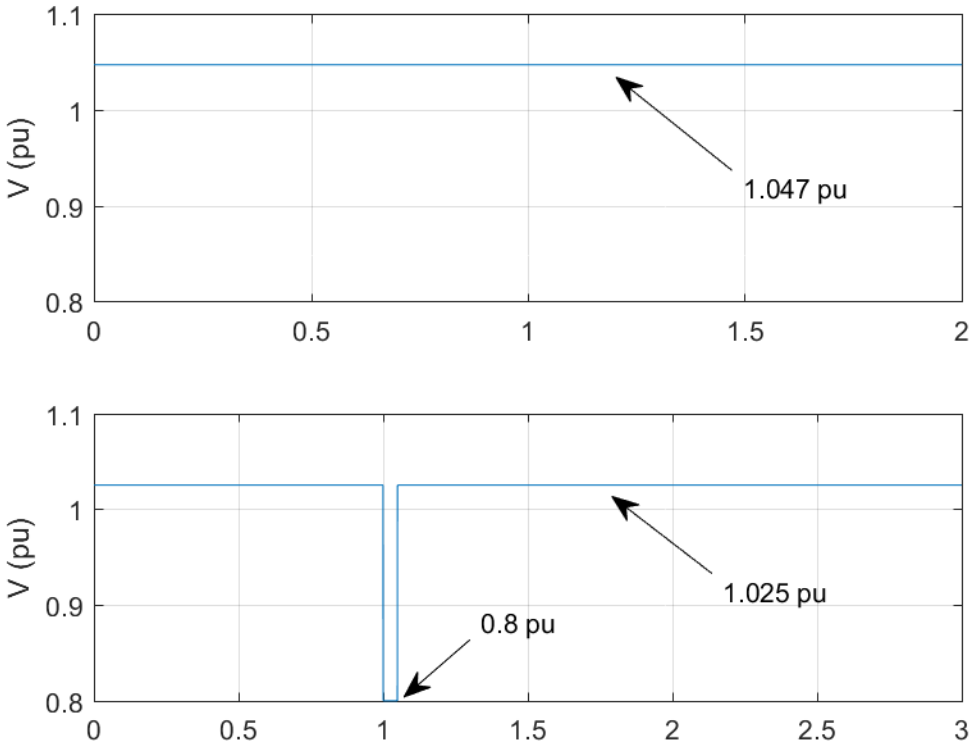


Figure 4: Voltage waveforms for Test 4.

3.0 Test Simulation Results:

The results of the test simulations listed above are shown in Appendix C. All the results were obtained using GE PSLF Version 21.0_03 release 8/9/17 with the beta version of *chvdc2*.

Appendix A – Parameter List for chvdc2

Parameter	Value	
dcbusr	17.000	
dcbusi	18.000	
MW_base	1000.000	
Talpr	0.020	
Kir	20.000	
Kpr	10.000	
alpha_max_ram	30.000	
Tram	0.100	
Vram	0.850	
Ttram	1.000	
maxc	0.015	
minc	-0.050	
rmax	10.000	
rmin	-10.000	
Tr	0.010	
Talpi	0.020	
Kii	20.000	
Kpi	10.000	
Kcos	0.070	
Kref	3.000	
Tref	0.010	
Kmax	0.150	
Tmax	0.010	
cosmin_i	0.956	
Imax1	0.100	
Imax2	1.000	
V1	0.250	
V2	1.150	
Tur	0.020	
Tdr	0.010	
Tui	0.030	
Tdi	0.010	
Flag	0.000	
Imax_lim	1.000	
Imin_lim	0.770	
max_err	0.500	
min_err	-0.500	
Tvd	0.250	
Vac_ref	0.960	
gamma_cf	0.000	
Tcf	0.034	
Vac_ucf	0.900	
Alpha_max_r	70.000	In GE PSLF these values are in the power flow cards; also dc margin is in Amps not pu as given here.
Alpha_min_r	5.000	
Idc_margin_r	0.000	
Alpha_min_i	110.000	
Idc_margin_i	0.100	

Appendix B – Tests Features

The test case is based on the CIGRE benchmark case [2] as a starting point, however, some significant changes were made for our purposes here.

1. The test case in [2] was primarily developed for use in electromagnetic transient (EMT) type programs and so has main circuit data (e.g. specific filter bank elements) which are not relevant to power flow and stability modeling (e.g. the filter banks are represented here as a fixed, lumped shunt capacitor, neglecting filter inductive and resistive elements).

2. The test case in [2] is based on a 50 Hz system, whereas the one here is a 60 Hz equivalent.

3. Some aspects of the model in [2] are not specified or pertinent to establishing a useful power flow and stability simulation set (e.g. MVA rating and parameters for equivalent generators for the two AC systems) and so these have been defined here using reasonable, assumed, values.

4. Some parameters were changed to result in a more simple and reasonable power flow solution for the test case used here (e.g. lumped capacitors used in [2] to emulate line charging are neglected, and some of the line parameters were rounded off etc.).

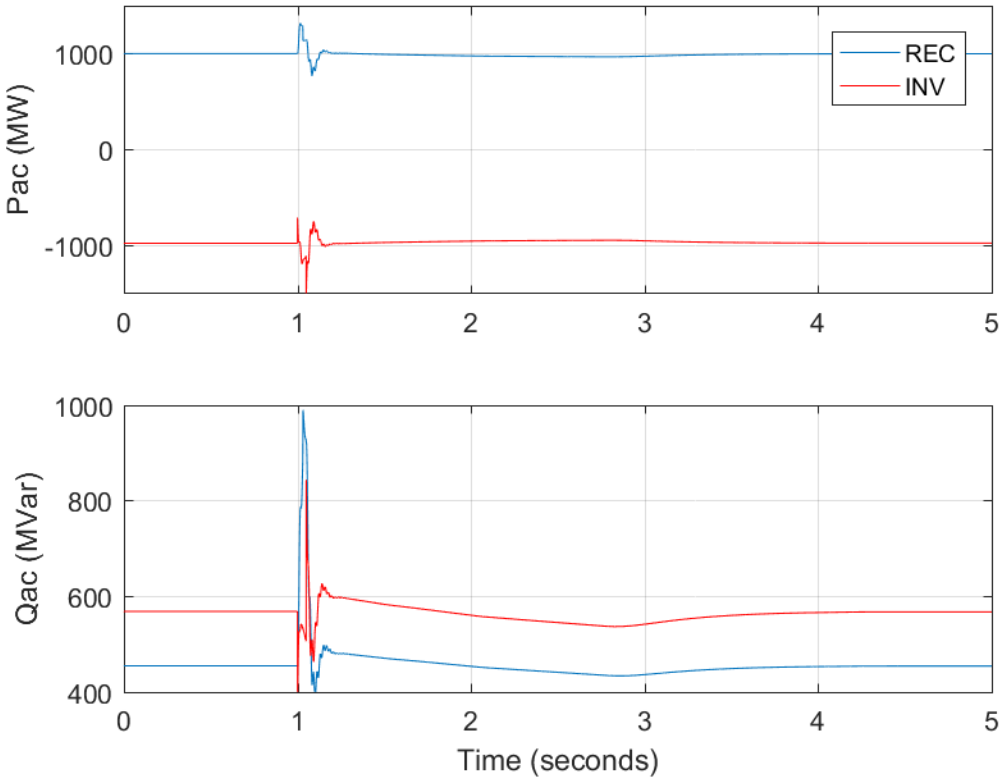
5. The power flow direction in our case here is reversed compared to [2]. This is not particularly of much importance or consequence, but should be noted (i.e. in the test case here the inverter is on the 345-kV side).

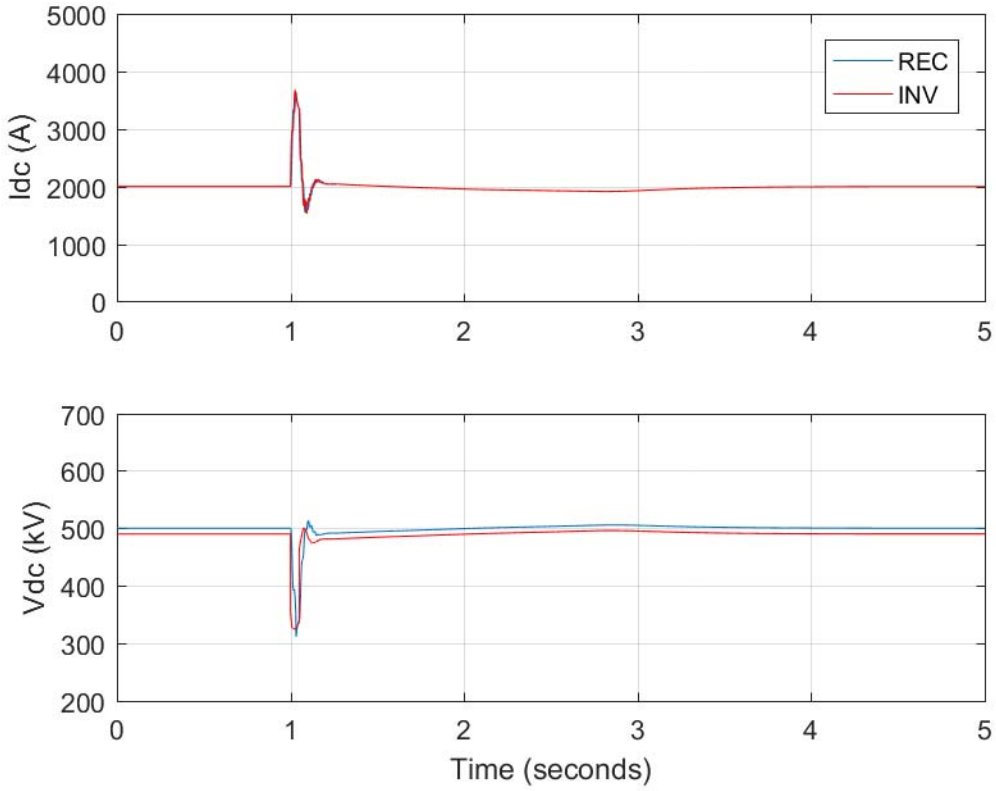
IMPORTANT DISCLAIMER:

The test case(s) presented here are only for the purpose of testing the proposed HVDC models and should not be viewed in any other context. It is not necessarily a realistic HVDC system.

Appendix C – Test Simulation Results

Test 1 – Inverter Side Fault

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Idc (A)
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Vdc (kV)
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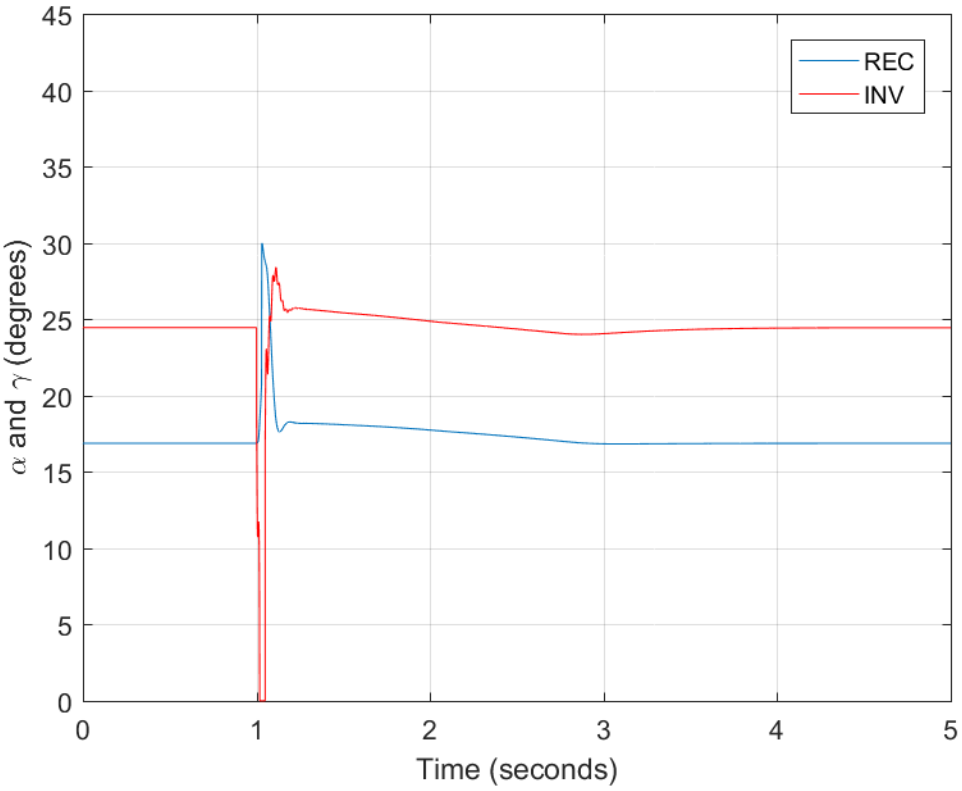
Time (seconds)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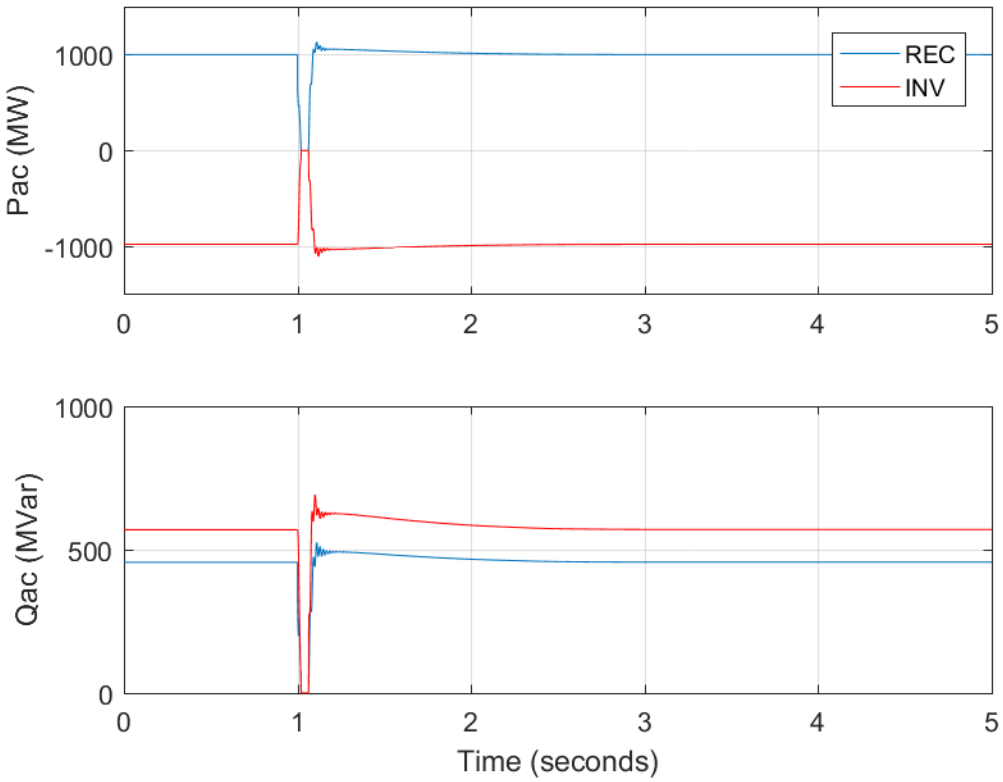
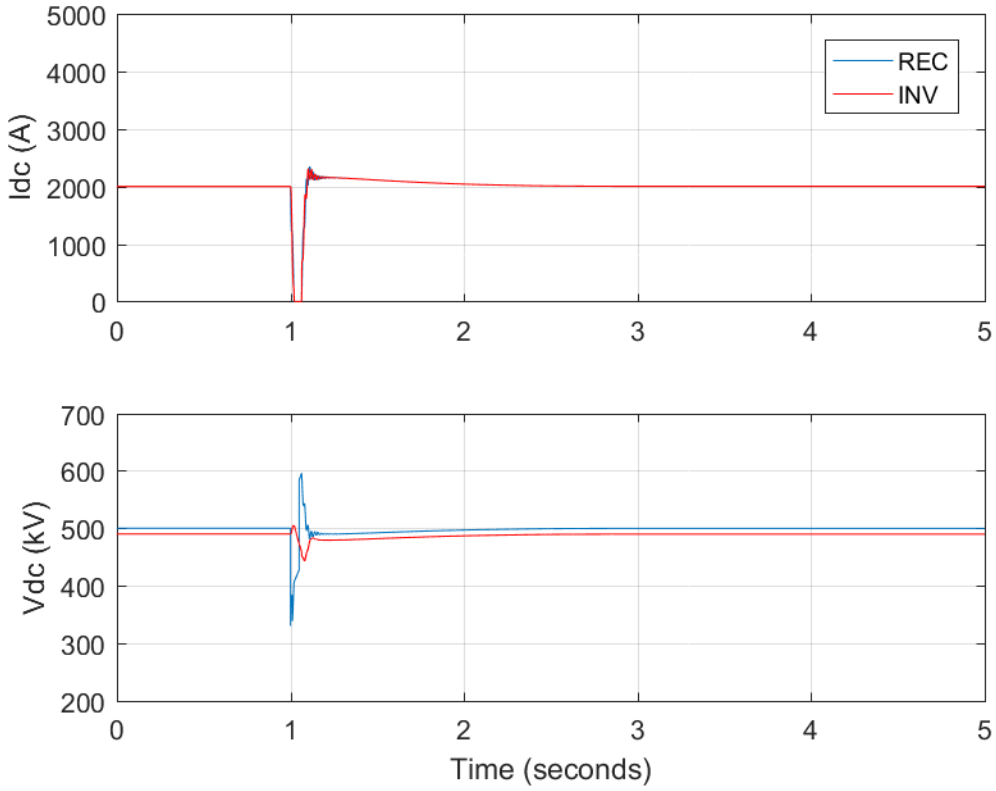
α and γ (degrees)
Time (seconds)
REC
INV

Test 2 – Rectifier Side Fault

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Vdc (kV)
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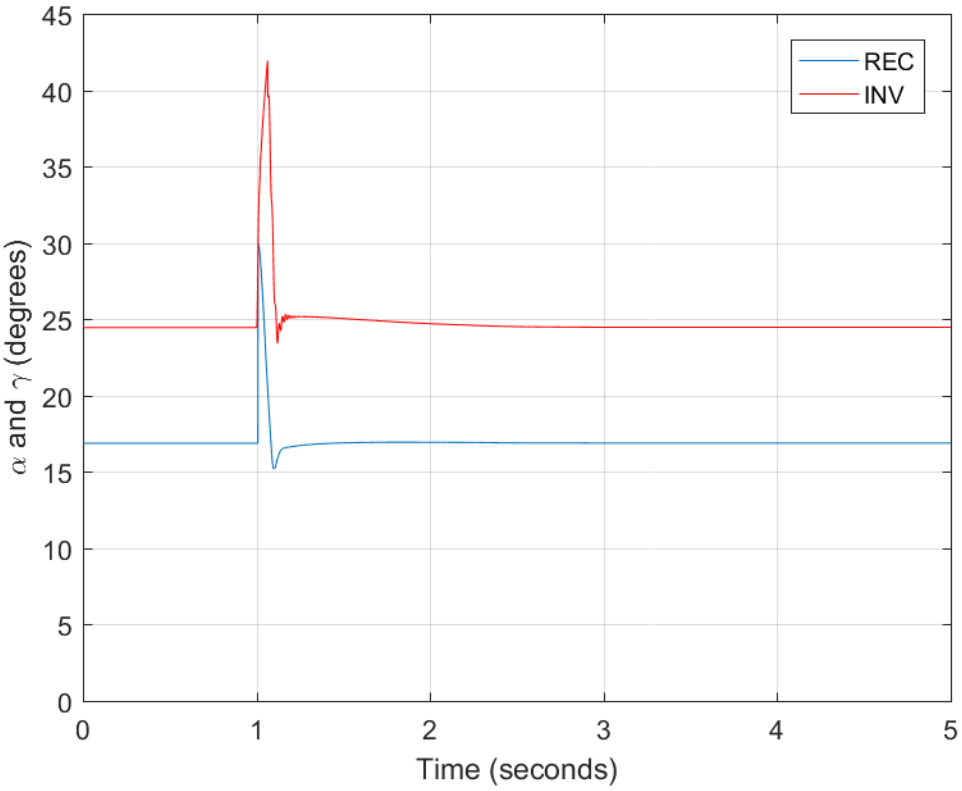
Time (seconds)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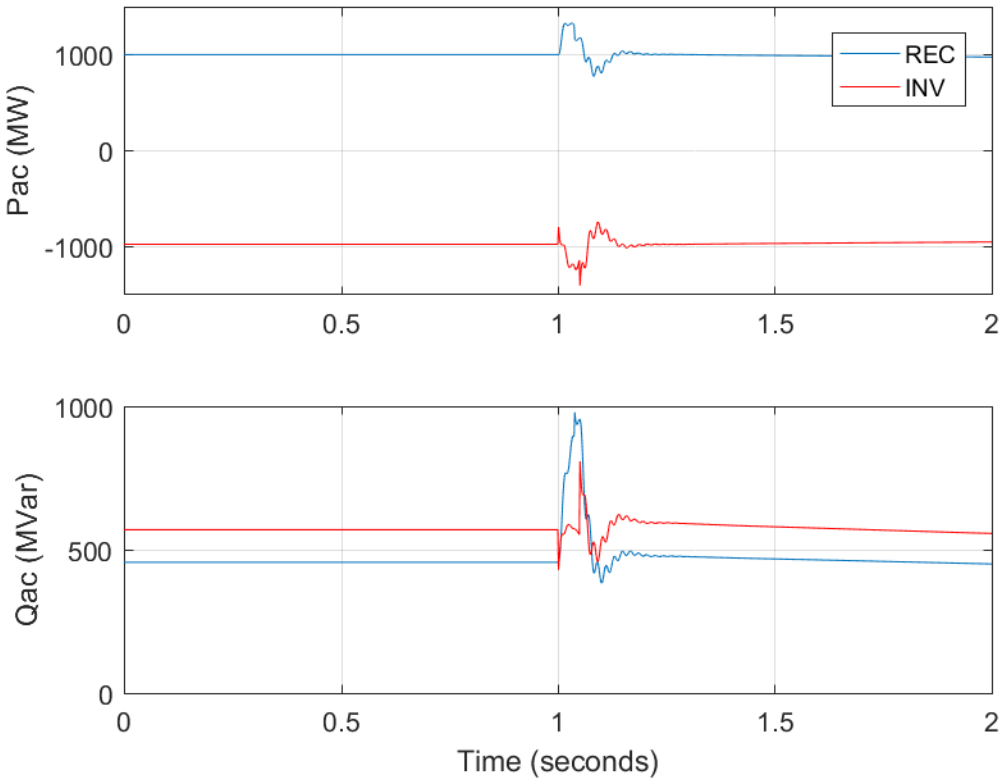
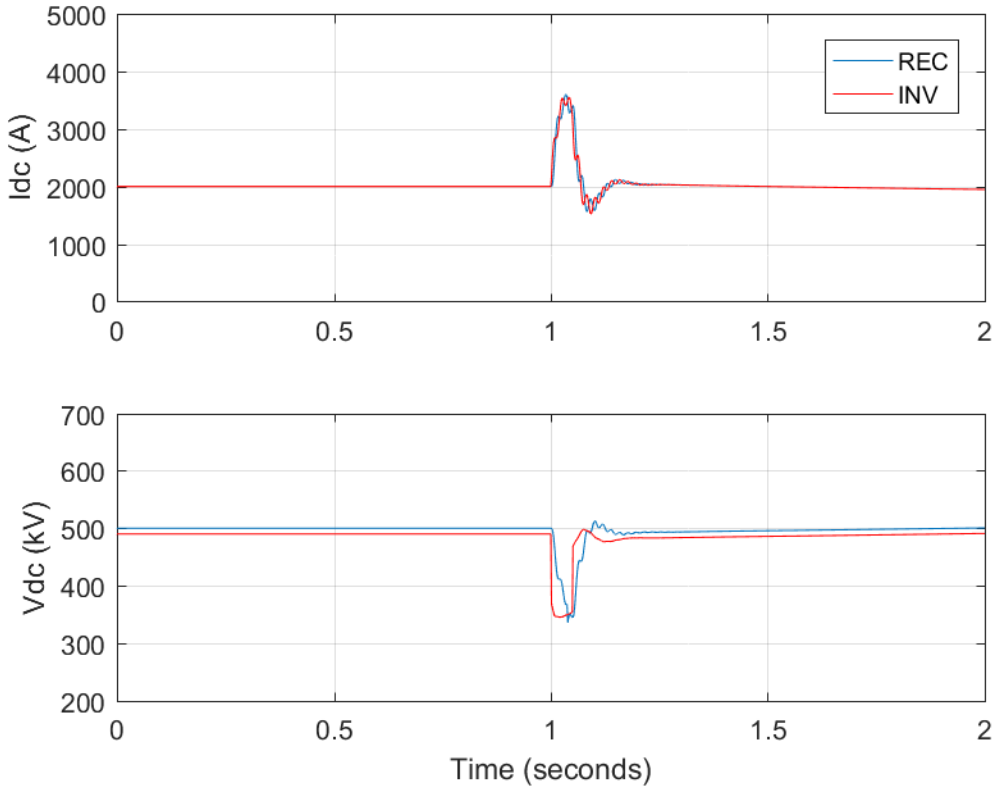
α and γ (degrees)
Time (seconds)
REC
INV

Test 3 – Inverter Side Voltage Playback

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Vdc (kV)
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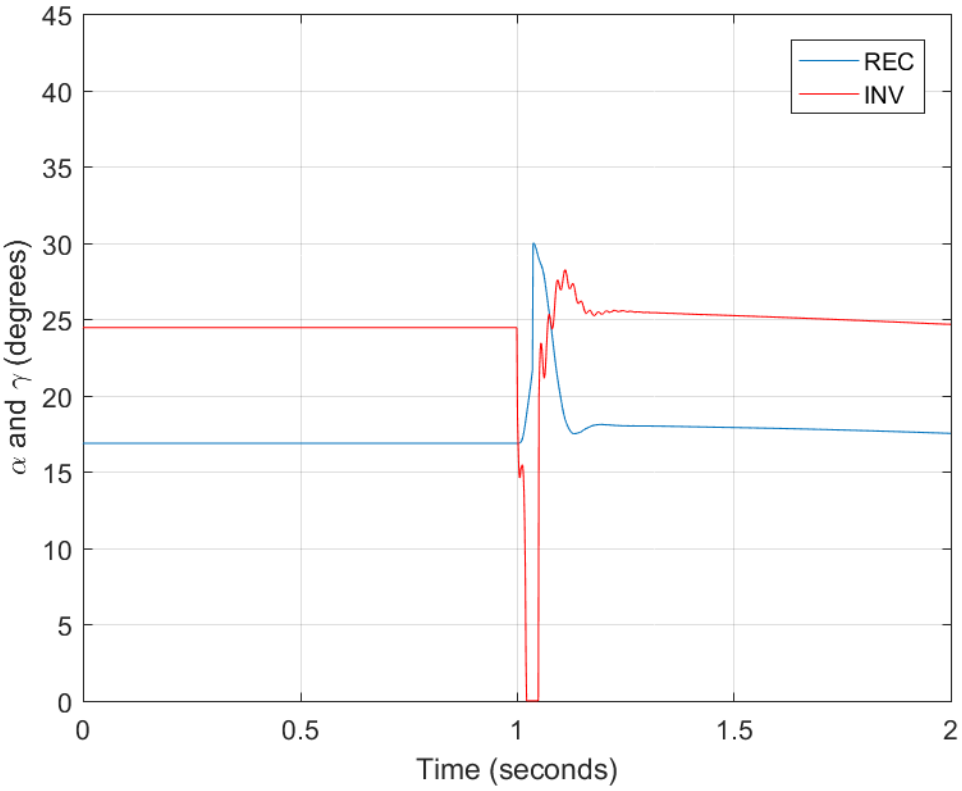
1.5
2
Time (seconds)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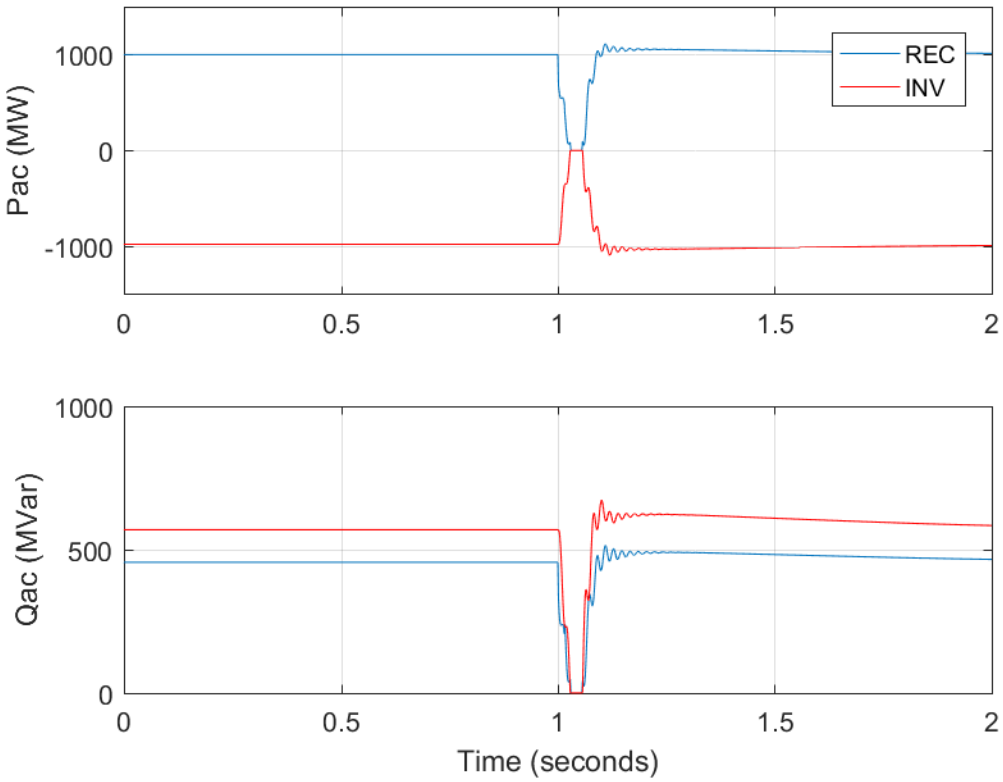
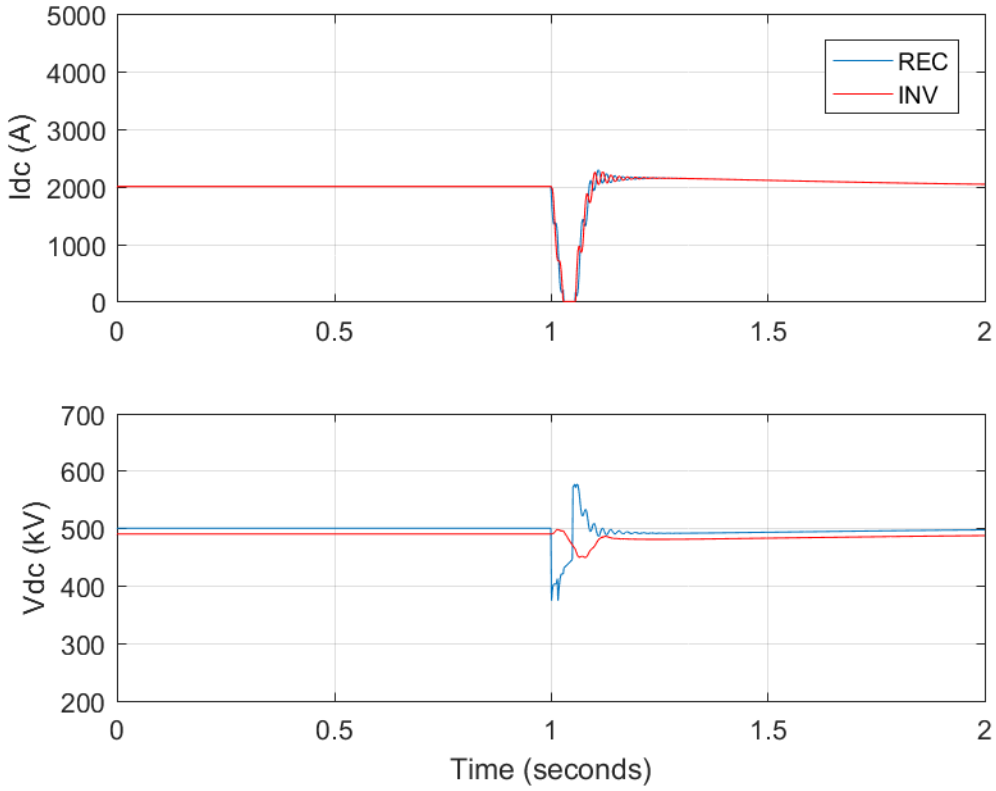
α and γ (degrees)
Time (seconds)
REC
INV

Test 4 – Rectifier Side Voltage Playback

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Vdc (kV)
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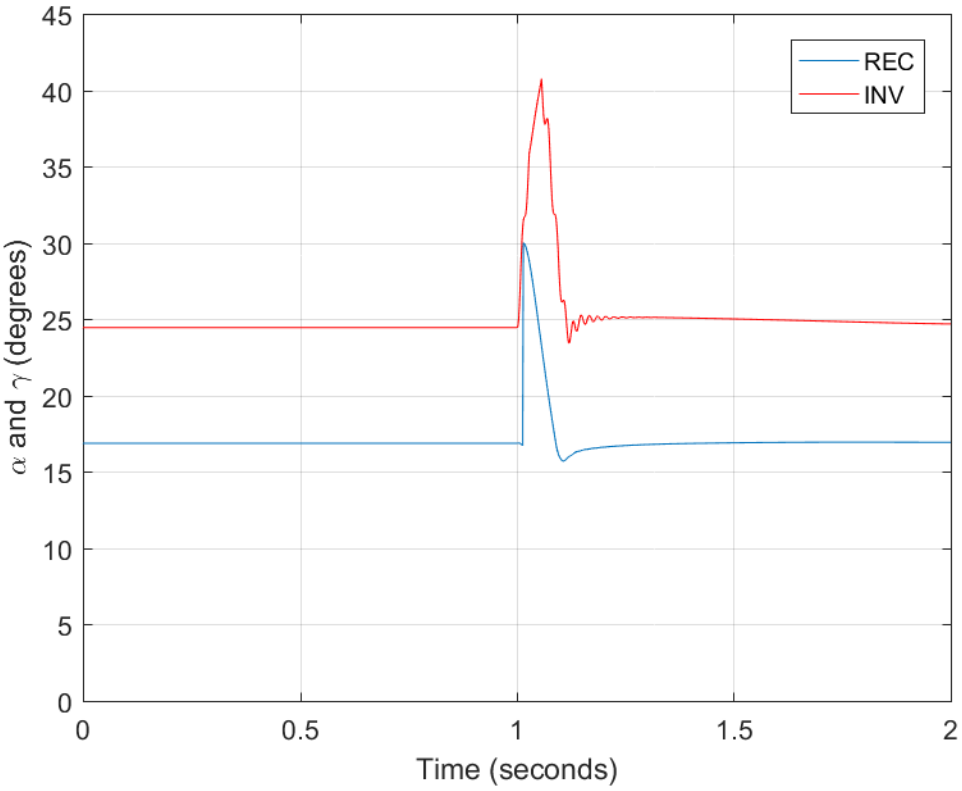
Time (seconds)



References:

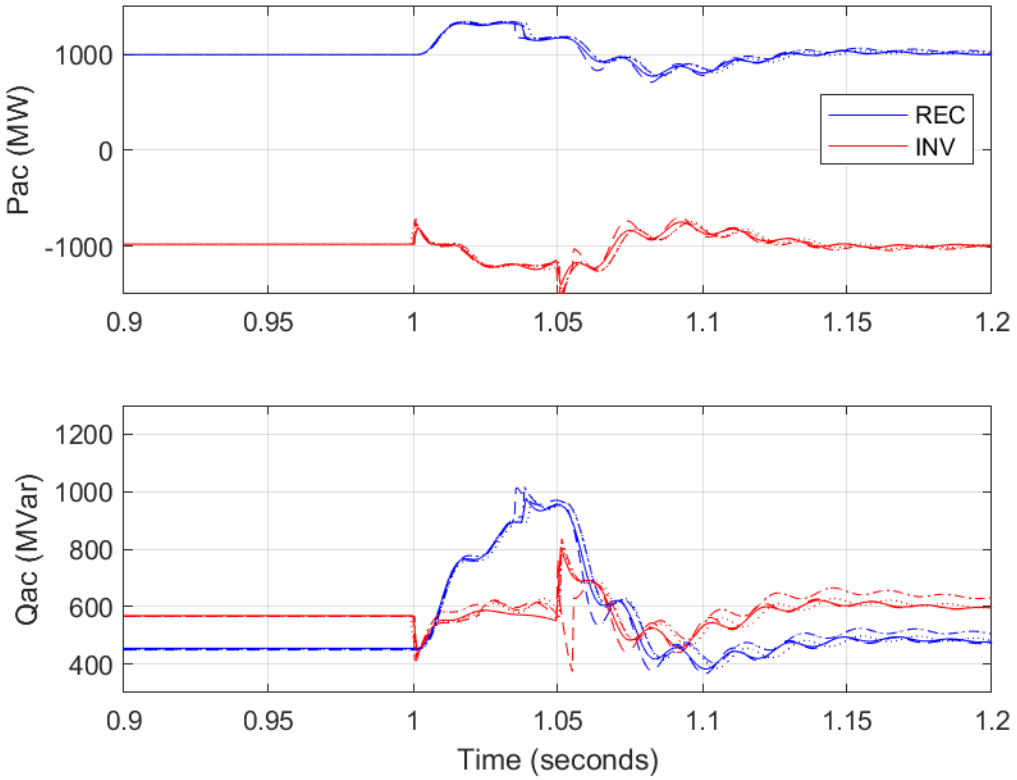
[1] P. Pourbeik, "Final proposed model specification for LCC HVDC", January 16, 2015 (revised 10/7/15; 10/30/15); issued to WECC HVDC Task Force and EPRI.

[2] M. Szechtman, T. Wess, C. V. Thio, H. Ring, L. Pilotto, P. Kuffel and K. Mayer, "First Benchmark Model for HVDC Control Studies", CIGRE Report of WG 14.02, Electra Magazine, 1991.

<u>Appendix D:</u> Comparison of the Simulations Across Four (4) Commercial Tools.

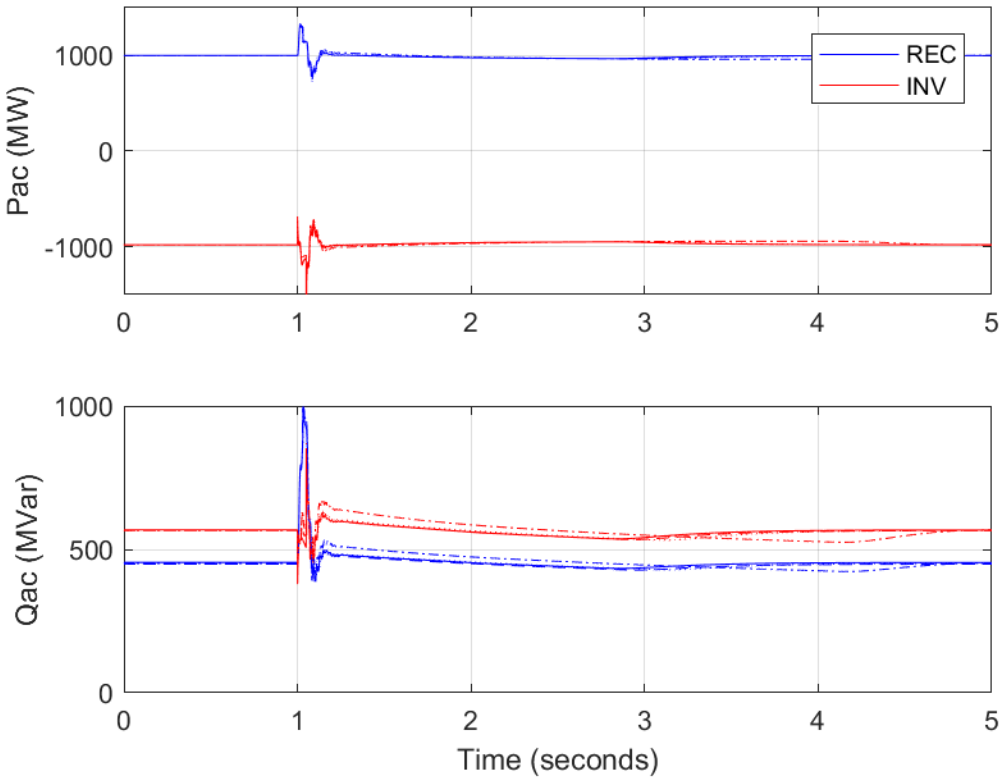
In all the plots below the SOLID lines are GE PSLF, the DOTTED lines are PowerWorld Simulator, the DASHED lines are PowerTech Labs TSAT™ and DOT-DASHED lines are Siemens PTI PSS®E.

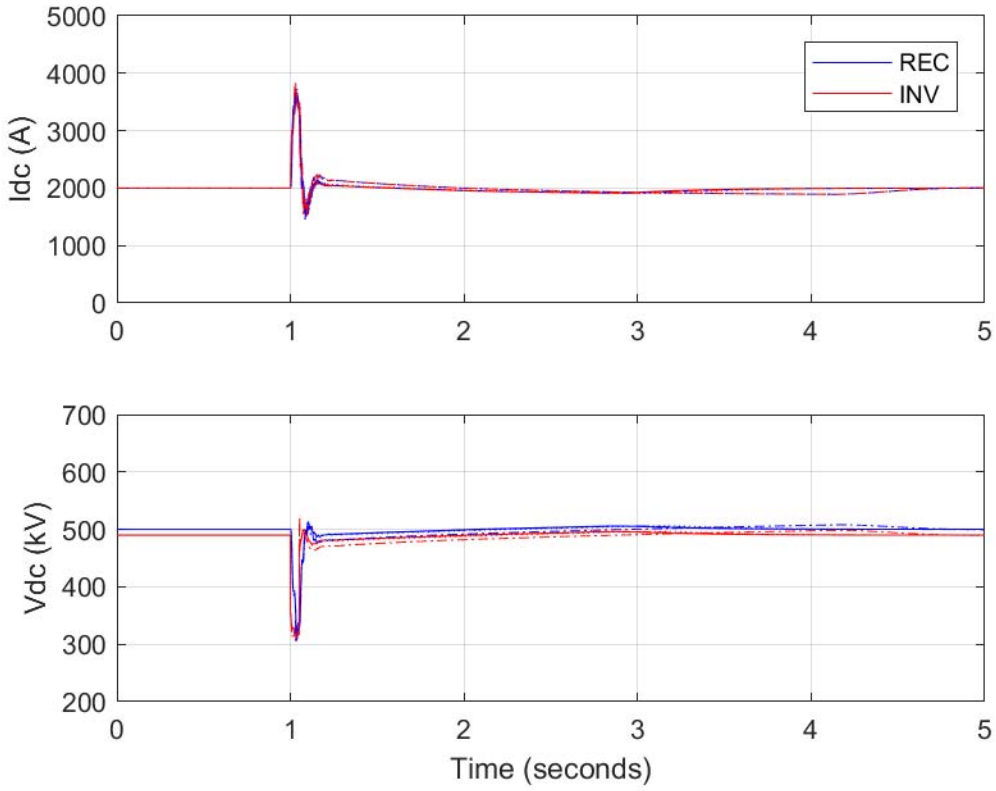
<u>Note:</u> it is difficult to see the difference between the lines below, because the results match quite closely across the four commercial software platforms. Below is a single example (expanded) plot to show that there is some small difference, but this is attributable to unavoidable numerical differences across different software.



Generally, as can be seen below there is very good agreement across all the commercial tools. Also, from the plots below it will be noticed that in Siemens PTI PSS®E, for the inverter side fault/voltage-play back, there is a slight mismatch in the value of firing angles following the event (and subsequently Q). In discussion with Siemens PTI, it is believed that this may be due to subtle differences in the dc-side solution of the line model. Siemens PTI will look further into this in due course and if subtle refinements might prove easy to implemented and to further improve the match, these actions will be taken in due course.

Test 1 – Inverter Side Fault

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Idc (A)
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Vdc (kV)
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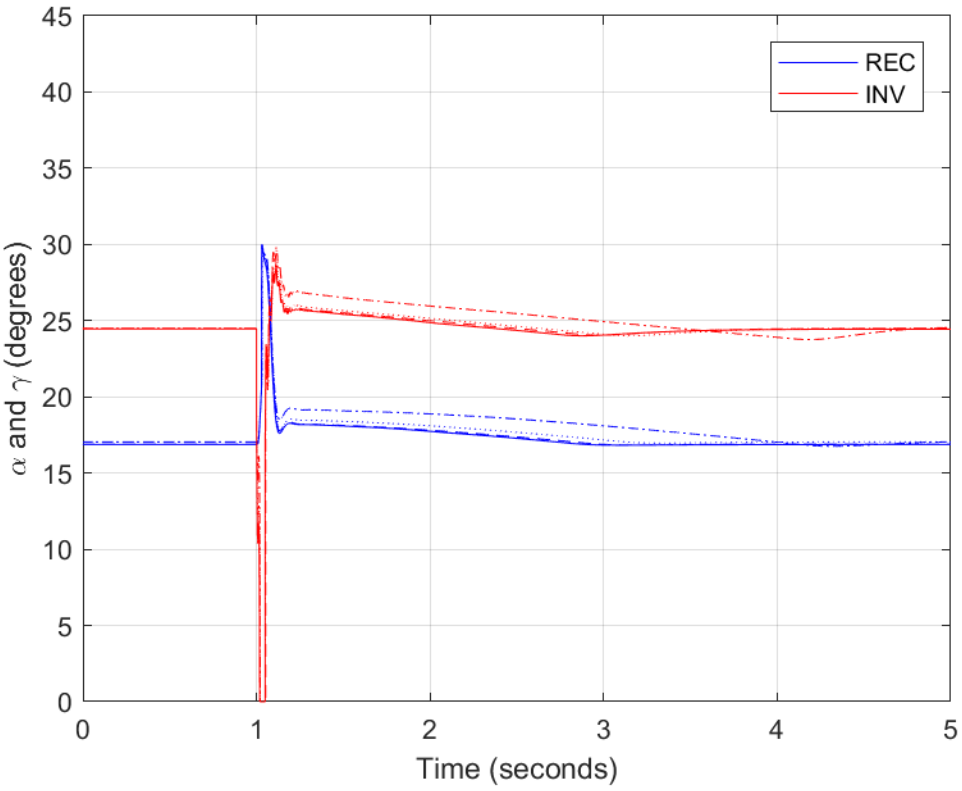
Time (seconds)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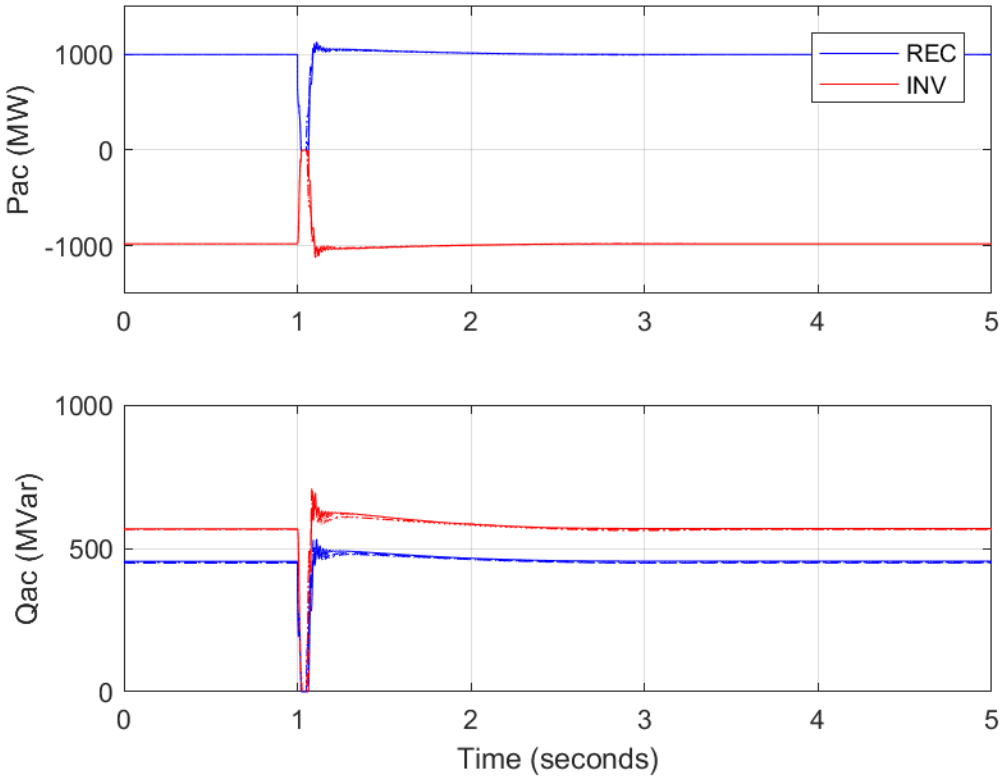
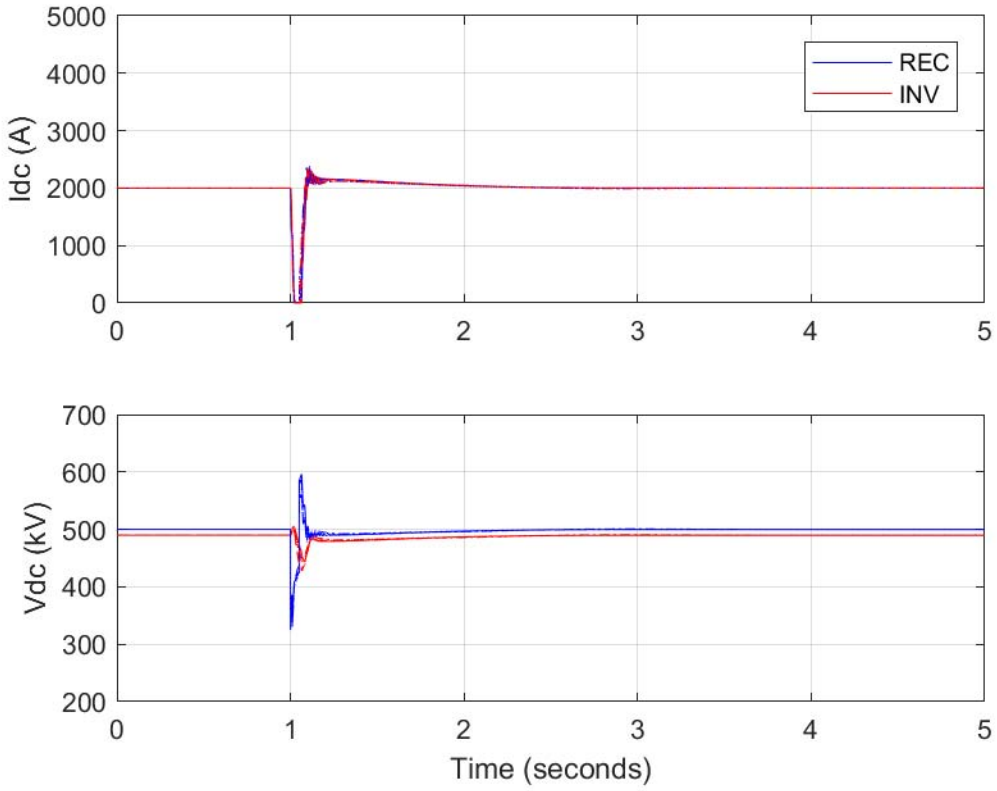
α and γ (degrees)
Time (seconds)

Test 2 – Rectifier Side Fault




Idc (A)
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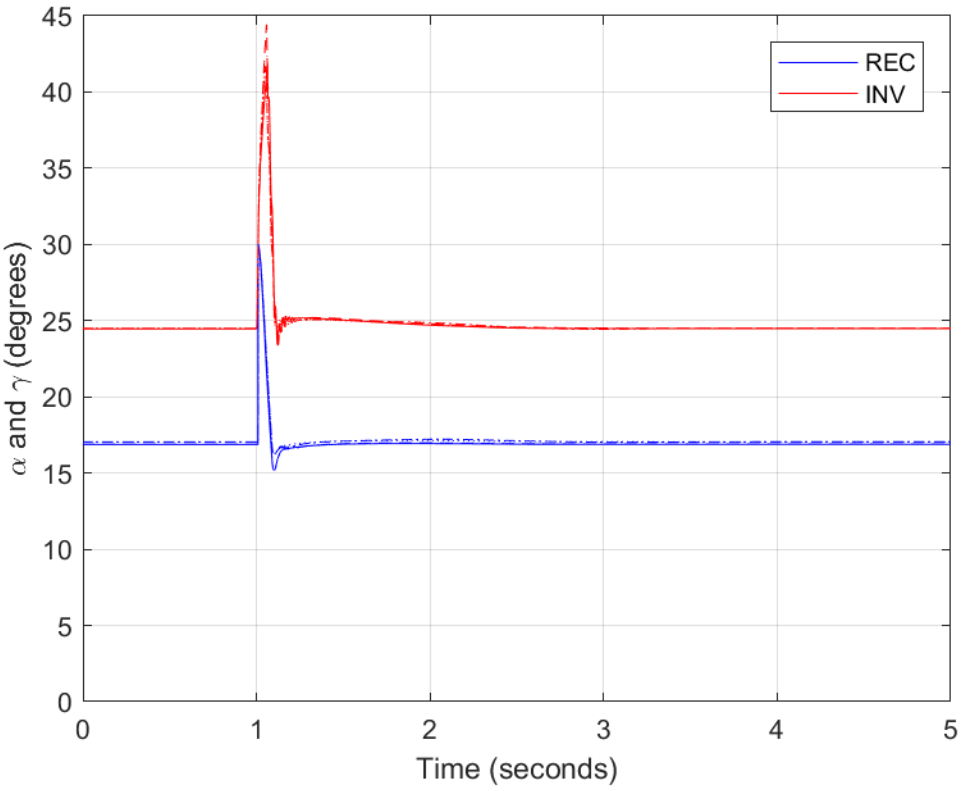
Time (seconds)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α and γ (degrees)
Time (seconds)
REC
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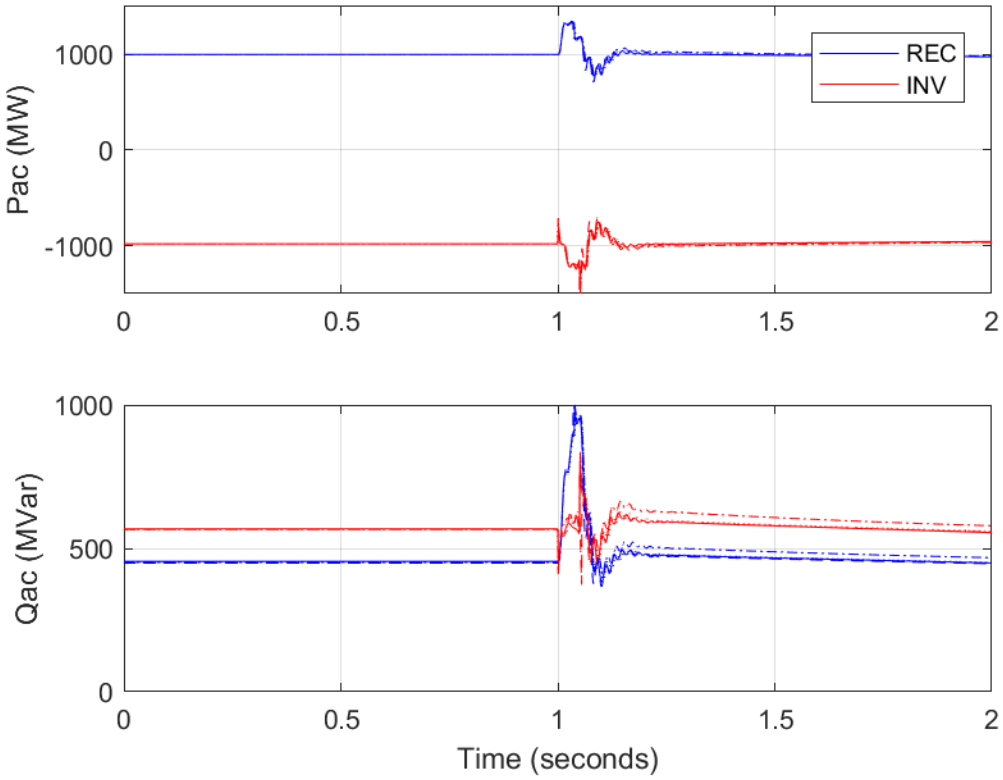
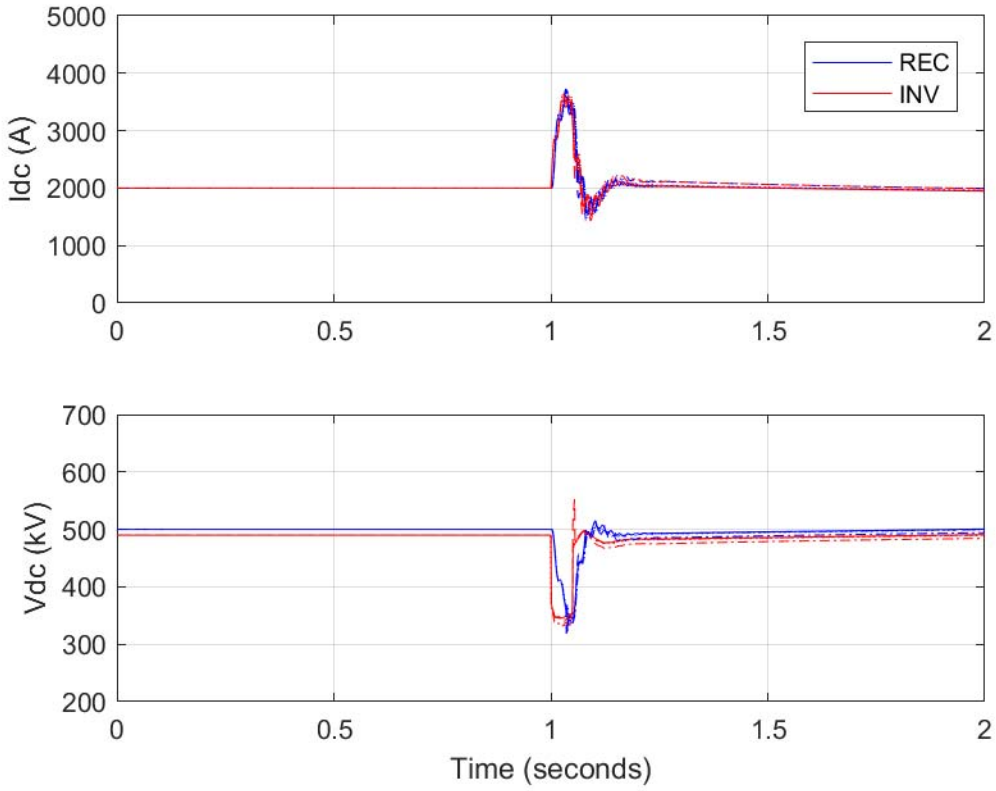
Test 3 – Inverter Side Voltage Playback

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Idc (A)
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Vdc (kV)
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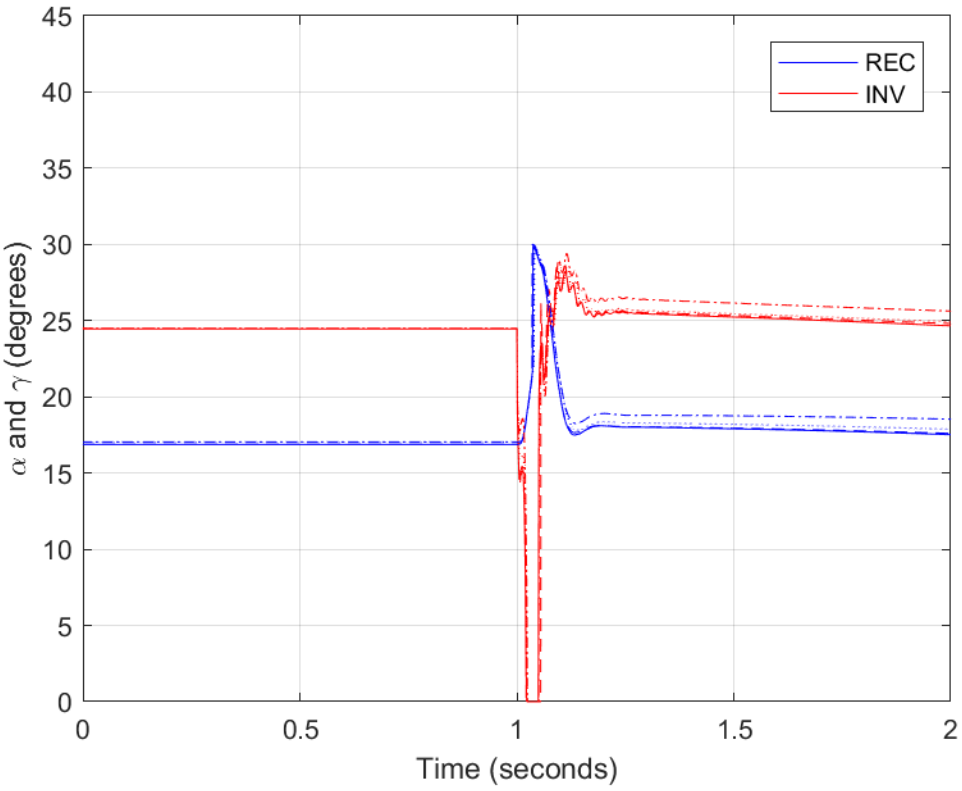
2
Time (seconds)


REC
INV
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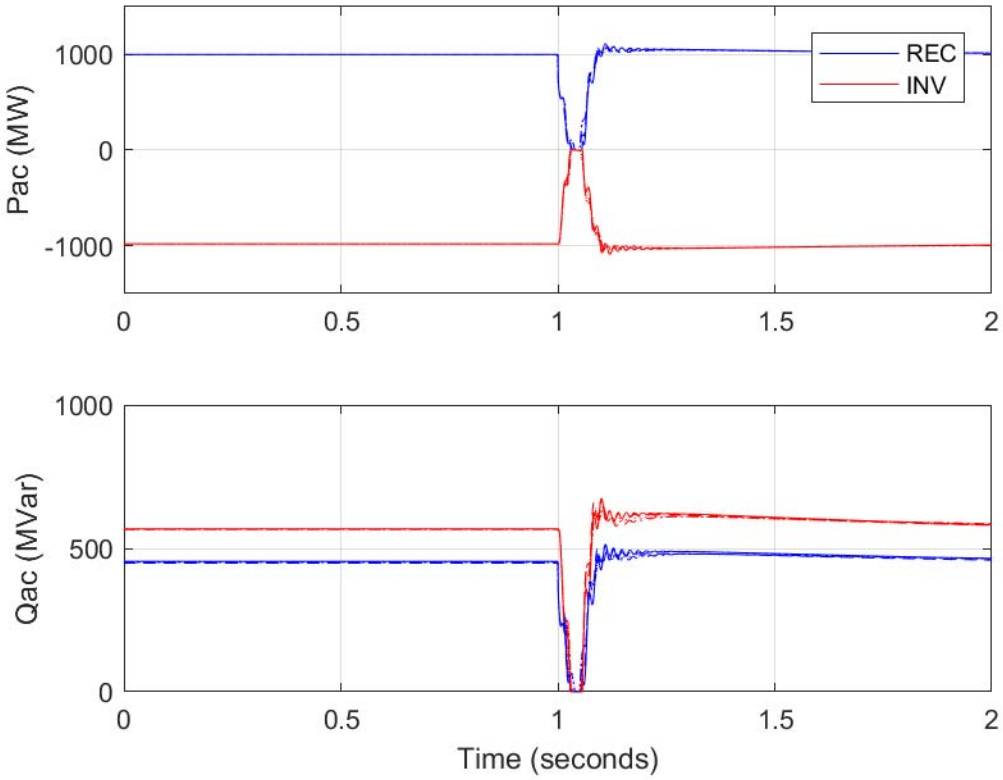
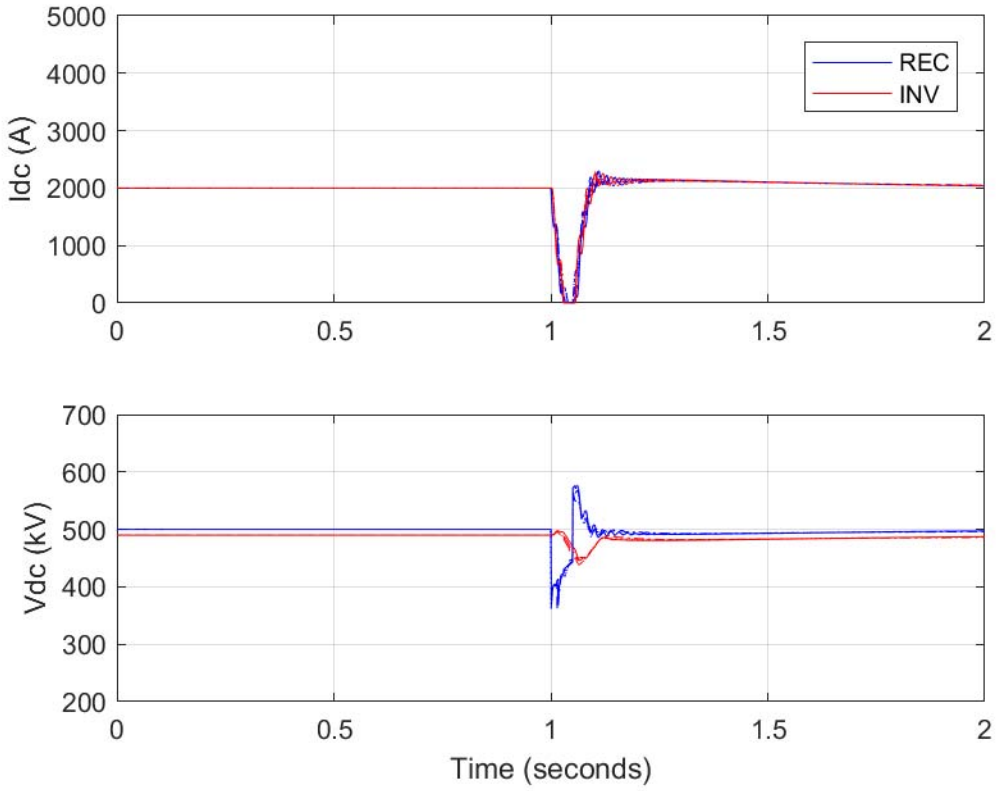
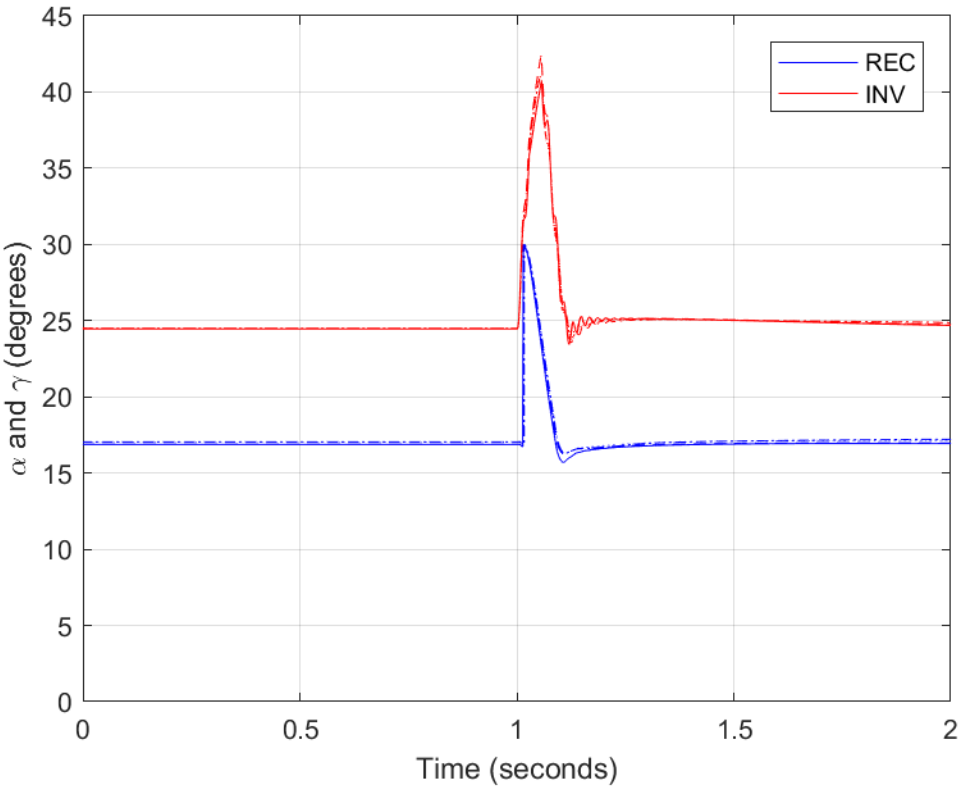
30
25
20
15
10
5
0
0
0.5
1
1.5
2
α and γ (degrees)
Time (seconds)

Test 4 – Rectifier Side Voltage Playback




5000
4000
3000
2000
1000
0
Idc (A)
REC
INV
0
0.5
1
1.5
2
700
600
500
400
300
200
Vdc (kV)
0
0.5
1
1.5
2
Time (seconds)


45
40
35
30
25
20
15
10
5
0
0
0.5
1
1.5
2
α and γ (degrees)
Time (seconds)
REC
INV