PROPOSED MODEL SPECIFICATION FOR SIMPLE VSC-HVDC

TO:	WECC HVDC TF & EPRI P40.016
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SUBJECT:	PROPOSED MODEL SPECIFICATION FOR SIMPLE VSC-HVDC
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CC:	ANISH GAIKWAD, EPRI

The WECC HVDC TF is working on developing simple planning models for both powerflow and dynamic time-domain simulations in positive sequence software tools for HVDC point-to-point transmission. Models are being developed for both conventional line commutated converter (LCC) HVDC and voltage source converter (VSC) technology.

The powerflow models for conventional HVDC have always existed in the commercial tools. In the past several years, the TF completed the definition of the VSC power-flow model, which has been implemented by the four major North American commercial power system simulation tools. In addition, in 2017 one of the two simple LCC-HVDC dynamic models (*chvdc2*) was also approved by WECC and has now been implemented and tested in the four major North American commercial tools (see https://www.wecc.biz/Administrative/Testing%20the%20chvdc2%20model.pdf).

This memo outlines the proposed simple VSC-HVDC dynamic model, the last of the tasks. It should be noted that this is a "simple" generic model for high-level stability studies and is NOT specific to any vendor, nor claims to have detailed vendor specific controls. Furthermore, the simple model presented here is intended for use in modeling point-to-point (not multi-terminal) VSC-HVDC that is imbedded within an existing AC network, and not for off-shore wind applications.

1.0 Voltage Source Converter HVDC Dynamic Model 1 (*vhvdc1*):

The proposed simple planning model 1 for a voltage source converter (VSC) HVDC is shown below in Figures 1 to 5. The model is intended to be a simple planning level non-vendor specific VSC-HVDC dynamic model for point-to-point transmission. A few high-level statements are pertinent:

a. The model is not necessary representative of any vendor or equipment. The control loops are "general" and "simple" proportional-integral (PI) control loops, on the assumptions that PI control is a common control strategy.

b. The volt/Var control loops (Figure 3) are intentionally quite similar to the high-level control-loop models in the *reec_a* model. This again is intentional, in order to give options of (i) voltage control with deadband/droop, or (ii) constant Q-control, or (iii) constant power-factor control.

c. The dc-line/cable is represented by a very simple model.

d. ***This is the first completed and tested version of the model.*** This was presented to the HVDC TF members (including all four major equipment vendors and commercial software vendors) on April 13th, in a webcast meeting, and later to the whole WECC MVWG at the

May meeting in Salt Lake City, UT. All typo and other minor comments received have been addressed. Two other substantial comments were presented:

i. All the equipment vendors indicated that this is a very simple model and although it may capture at a high-level the concepts and performance of VSC-HVDC, it does not capture the nuances of actual equipment. This is of course already acknowledged in item a. above. Again, it is emphasized that the intent here is to have a simple, transparent and transportable (i.e. model that is standard across the major software platforms) model. Vendor specific, detailed models will always be needed for detailed local studies.

ii. One equipment vendor suggested that a more detailed dc-line model may be useful. Since no further information was received after this comment on the call, no further action was taken. Again, it is emphasized that although there is certainly not a "perfect" match, none-the-less, the parameterized simple model presented here gives a "reasonable" emulation of the performance of a user-written vendor specific model as shown in section 2.1 below.

iii. Some other high-level comments were also made by another vendor about potential future functionalities to consider for the model – e.g. voltage dependent reactive limits. Again, however, since further details were not provided, this is not considered in this version of the model.

Participants in the April 13th WECC HVDC TF webcast were ABB, Siemens, GE, Mitsubishi, Siemens PTI, PowerWorld, Powertech Labs, EPRI, PEACE®, BPA and PacifiCorp.

As an initial test of the concept, the model was implemented in GE PSLF™, as a user-written model. The results of the testing are shown in section 2.0.

First some of the salient points, and assumptions, in proposing this model should be listed:

1. The intent of the model is for planning studies in positive-sequence programs such as GE PSLF™, Siemens PIT PSS®E, PowerWorld Simulator and PowerTech Labs TSAT™, and other similar tools. Thus, it should be understood that the model is not appropriate for studying the details of converter response and design to unbalanced disturbances.

2. Following on from point 1 above, this model is not intended, nor adequate, for studying the details of DC side faults. The dc-line (cable) dynamics model is rather rudimentary. Furthermore, positive sequence simulation platforms are likely not the best tool for studying dc-side phenomena.

3. At the moment, to our knowledge[1], none of the commercial tools allow a seamless link between the VSC powerflow and dynamic models (as is the case for LCC-HVDC). That is, in order to develop and test the user-written model we had to place two "fictitious" generator models in the power flow case at the respective rectifier and inverter ends of the point-to-point HVDC transmission and then link the user-written model (through the *vscdc* model in

[1] Certainly, true for GE PSLF™, and likely true for the other commercial tools, thought we cannot say with absolute certainty.

GE PSLF™) to the two generators. The model then emulates everything shown and discussed here, and injects, at every time step, the appropriate ac real and reactive power at the terminals of each of these fictitious generators to emulate the converter response. Once the model is agreed upon, for the final implementation in the commercial tools, should the software vendors graciously agreed to adopt the model, the following is suggested:

a. The model should link to the power flow VSC-HVDC model, similar to the LCC-HVDC dynamic models.

b. The converter interface should be modeled as a voltage-source, i.e. similar to the existing *vscdc1* model in GE PSLF™, i.e. a voltage-source with source impedance of Xe.

4. The model has the following salient features:

a. A simple model of the dc-line/cable dynamics as shown in Figure 1. This is necessary to capture the basic behavior of the dc voltage and current.

b. A PI control loop controlling the dc voltage and a PI control loop controlling the dc current, as shown in Figure 2.

c. **Each converter** has a voltage/Q controller as shown in Figure 3. This allows for several control options:

i. Voltage control with deadband (*dbd1*) and/or reactive droop (*Kc*), when *Refflag* = 1

ii. Constant Q control with deadband (*dbd2*), when *Refflag* = 0

iii. Constant power factor control with deadband (*dbd2*), when *Refflag* = 2

d. The six (6) point piece-wise linear curve defined in Figure 4, allows an emulation of the reduction on the maximum allowable power reference (*Pmax*) as a function of the available ac voltage. That is, this function acts to dynamically change *Pmax* as shown in Figure 2. This is defined by the ten (10) parameters, *P1, P2, P3, P4, V1, V2, V3, V4, V5* and *V6*.

e. The current capability of the converters is modeled by a simple capability-curve as shown in Figure 5, and defined by the eight (8) parameters, *Imax, Ipmax1, Ipmax2, Ipmax3, Iqmax2, Iqmax3, Iqmin2* and *Iqmin3*. Thus, independently, **on each** converter the current *Ip* (active current being injected into the grid) is calculated at every time step and thus based on the current value of *Ip, Iqmax/Iqmin* is determined from this capability-curve, and subsequently *Qmax/Qmin* is calculated as the value of *Iqmax* × *MWrating* and *Iqmin* × *MWrating*. Thus, real and reactive power are independently controlled on either side of the HVDC link, within the current ratings of the

converter. Note that inherently the HVDC link is always in P-priority[2] – that is, real power always takes precedence.

f. No transducer time-constants have been modeled associated with the measurement of the dc quantities on the dc-side in the controls, since it is assumed that dc voltage and current are likely measured directly with a voltage-dividers and a shunt and thus there is no appreciable measurement time.

g. **Rudimentary Protection Emulation:** Also included in the model is a simple representation of converter blocking for severe nearby ac faults. Each converter has its own blocking function, and the logic is as follows:

```
If Vac ≤ V_block
        Block = 1
Endif

If (Block = 1)
    If ( (Vac ≥ V_unblock) and Start_Unblock_Timer = 0) )
        Unblock_Timer = current_simulation_time
        Start_Unblock_Timer = 1
    Endif

    If ( (Start_Unblock_Timer = 1) and (current_simulation_time – Unblock_Timer ≥ PLL_delay) )
        Unblock_Timer = 99999
        Start_Unblock_Timer = 0
        Block = 0
    Endif
Endif
```

The above is applied separately to both the rectifier and inverter side converters; thus, we have *Block_rec*, *Block_inv*, etc. Then the following logic is applied at the appropriate place in the code:

```
If (Block_rec = 1) or (Block_inv = 1)
    Pref = 0
Endif

If (Block_rec = 1)
    Qac_cmd_rec = 0
Endif

If (Block_inv = 1)
    Qac_cmd_inv = 0
Endif
```

[2] After initial discussion with vendors, there might be a need/desire to offer the possibility of Q-priority also in this simple model. This is to be further discussed in the future.

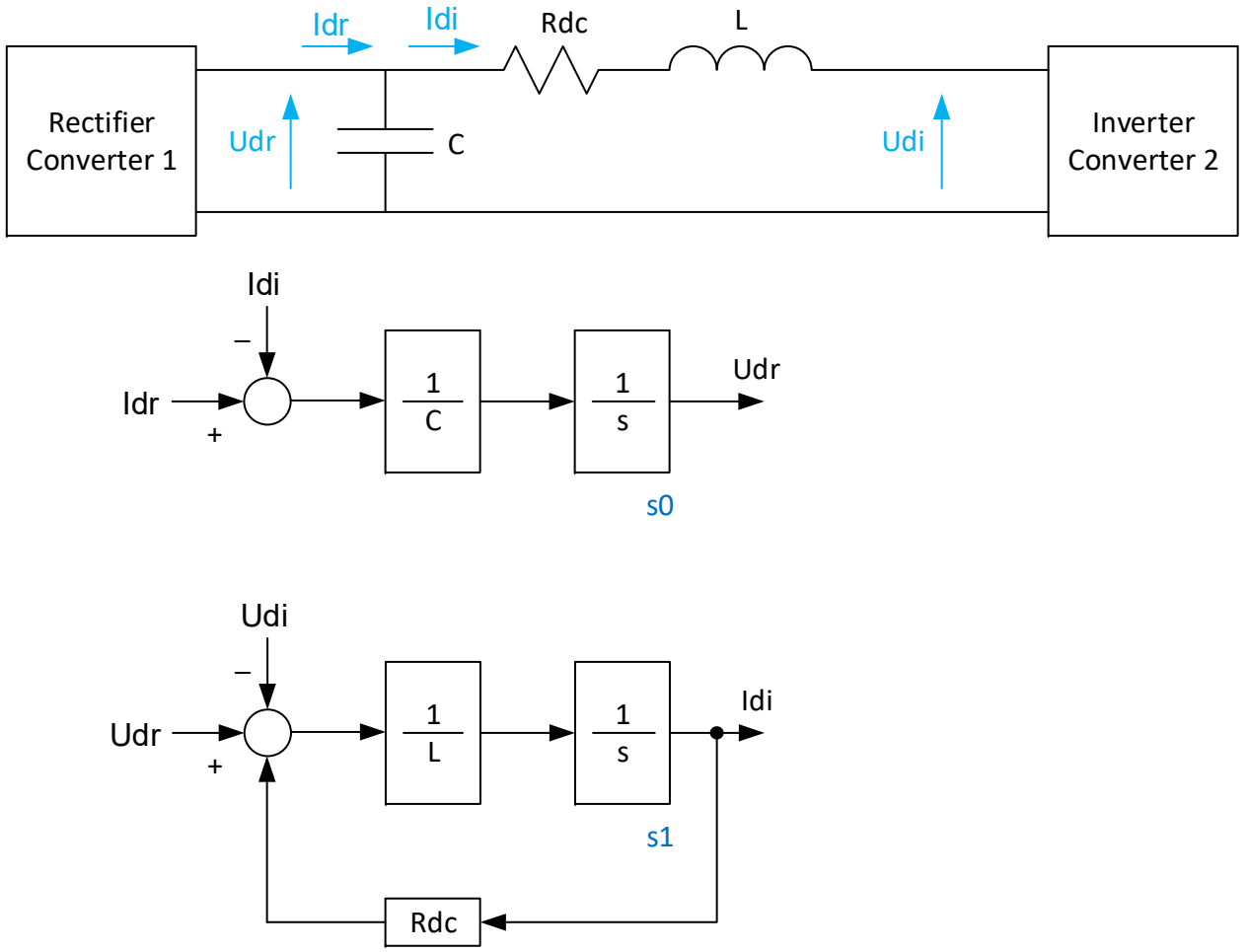

Figure 1: Simple, proposed, dc-line dynamics.

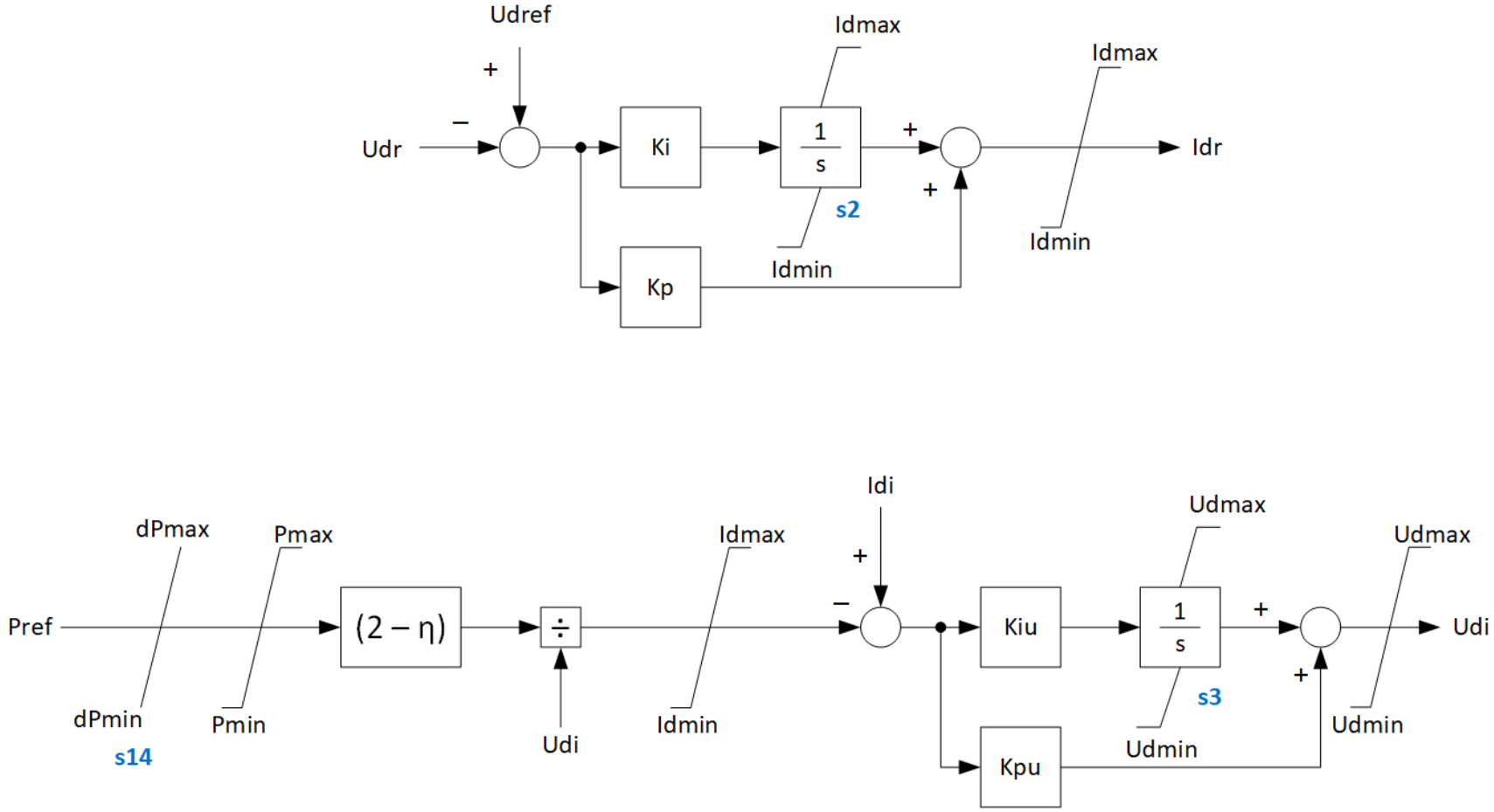

Figure 2: Dc current (Idr) and voltage (Udi) control.

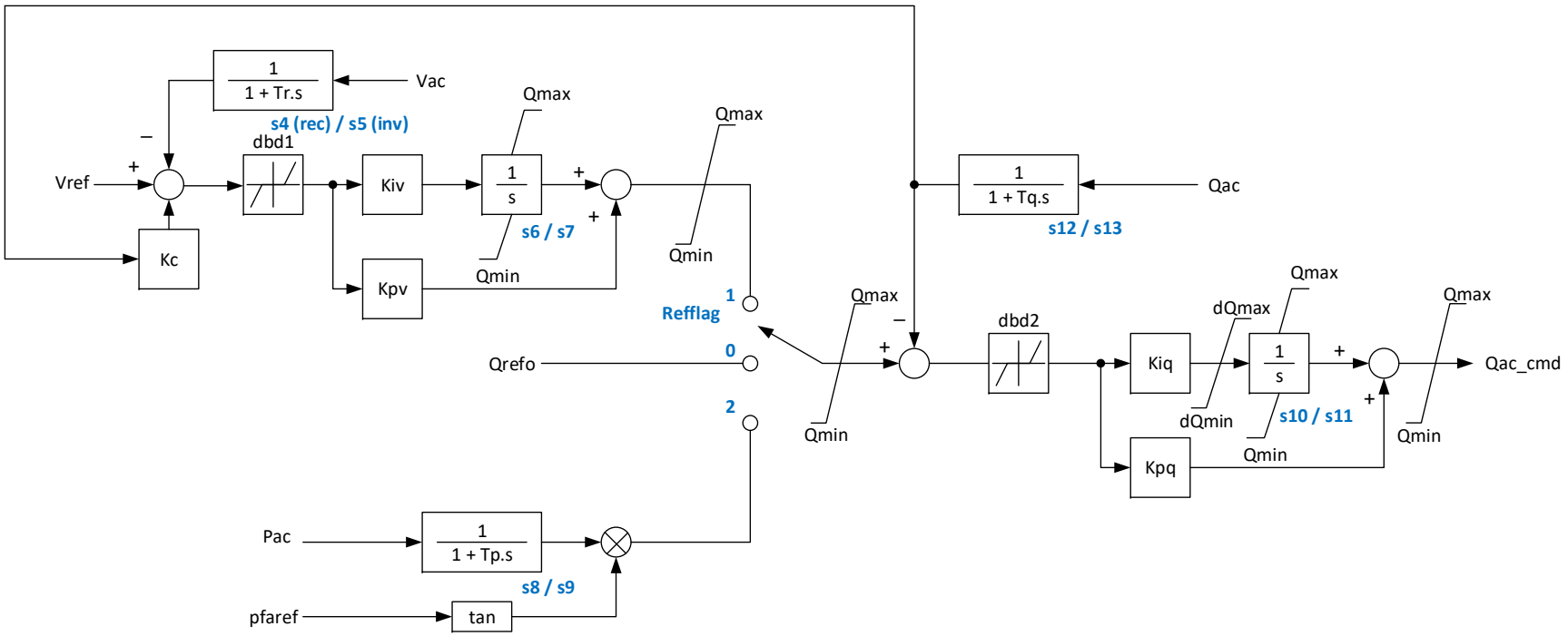

Figure 3: Volt/Var Controls on each converter.

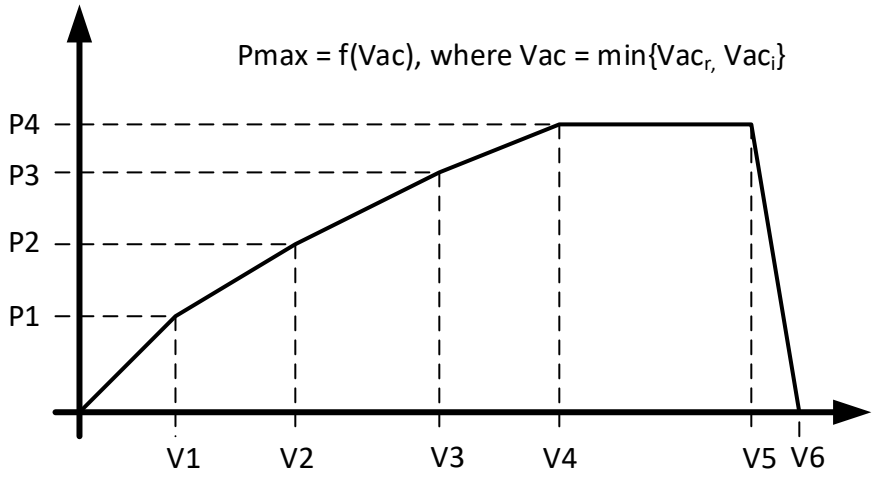

Figure 4: Power versus Voltage look-up table/curve for defining the maximum dc power reference as a function of ac voltage.

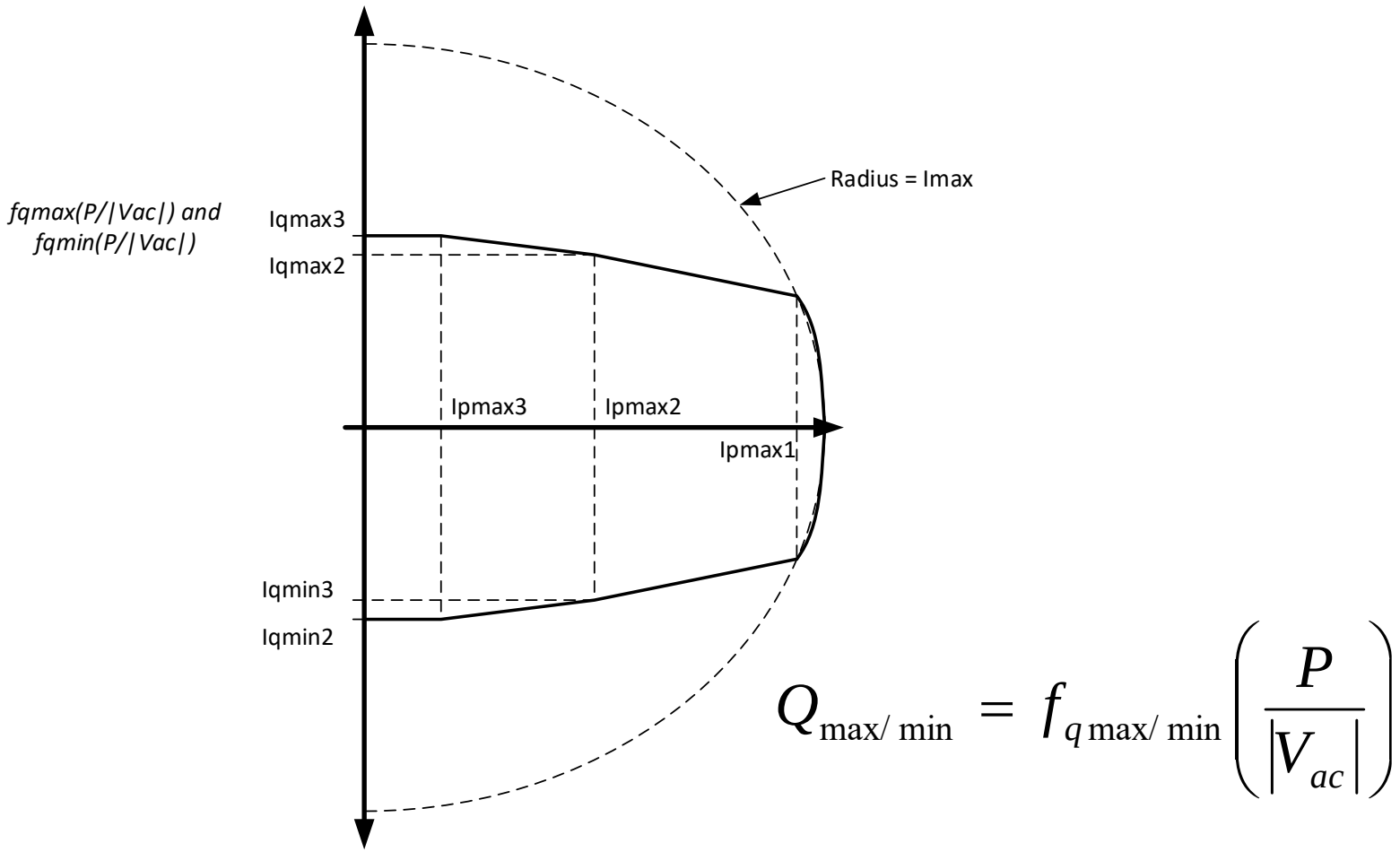

Figure 5: Definition of the reactive power capability of both converters (D-curve) as a function of dc power transferred and ac voltage.

2.0 Testing the Model:

2.1 Test Case 1 – WECC Case and Comparison to User-Written Vendor Model:

The first test case we ran was to make a high-level attempt to tune the model parameters to emulate the response of the vendor developed user-written model of the TBC VSC-HVDC system that presently exists in the WECC GE PSLF™ base cases. There is no doubt that the vendor developed user-written model for TBC is somewhat more complicated and very different than the simple proposed VSC-HVDC model (*vhvdc1*) presented here. However, at a high-level it has similar features, i.e.:

1. A simple dc-cable model, similar, if not almost identical to the one presented here. The model has a lumped R, L and C defined as input parameters.

2. Closed loop proportional-integral (though implemented quite differently) controls around power reference and dc-voltage control.

3. Independent volt/var control on each converter.

4. A ac-voltage dependent power reference limit.

5. A sophisticated (significantly more complex) Qmax/Qmin determination based on active power transfer etc.

It can thus be seen from the above that our proposed simple *vhvdc1* model has all of these features, however, likely some of them are more "generic" and simple. None-the-less, the following was done:

- A simple test case was set-up by creating a reduced WECC case around the two ends of the TBC VSC-HVDC system.

- The *vhvdc1* model was then parameterized by:

    - Taking those parameters that could easily be extracted from the TBC vendor model (e.g. cable R, L, C, etc.)

    - Fitting other parameters through an iterative process and using some engineering judgement.

We then ran the following simulations on the test case using both the original vendor specific user-written model for TBC and the parameterized *vhvdc1* model.

Table 1: Test simulations

Simulation	TBC Vendor Specific Model	Parameterized vhvdc1 model
X=0.01 pu fault on Rectifier side	test1	testg1
X=0.001 pu fault on Rectifier side	test2	testg2
X=0.01 pu fault on Inverter side	test3	testg3
X=0.001 pu fault on Inverter side	test4	testg4

The simulations results are shown in Figures 6, 7, 8 and 9, below, respectively.

From the results presented below, the following conclusions may be drawn:

1. ***Disclaimer*** – it is NOT being claimed here that the parameterized *vhvdc1* model is an exact or faithful match of the vendor-specific user-written model, nor that it can necessarily be used in place of that model for any studies. The results here are rudimentary and of only a few sample simulations. Much more work would be needed to see if it behaves well under numerous other conditions. Even then, it is still not being claimed here that it could replace the vendor-specific model for any local-studies.

2. The above disclaimer aside, one can see from the simulations below that the *vhvdc1* model, once reasonably parameterized, provides a reasonable response to the ac faults that reasonably emulate the behavior of the detailed vendor-specific model. In summary:

    a. For remote faults we see as might be expected a dip in the MW transfer of the line, due to a change in the power reference as a function of the ac voltage dip.

    b. For close-in faults we see the blocking of the associated converter and thus the power transfer dropping to zero and then ramping back up, after the fault clears.

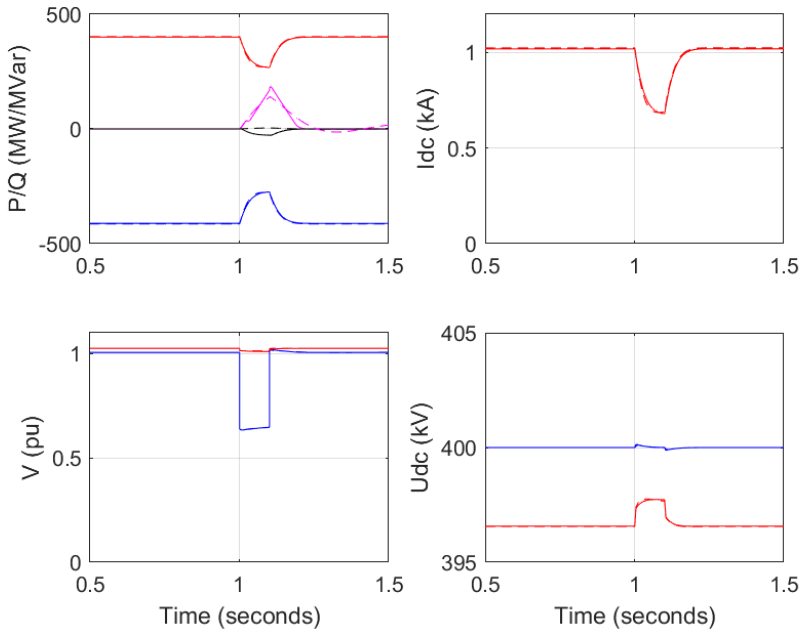

Figure 6: Remote rectifier side ac fault. **Blue** lines are rectifier quantities. **Red** lines are inverter quantities. **Solid** lines are the user-written vendor specific model. **Dashed** lines are the simple-generic vhvdc1 model, reasonably parameterized, as presented here.

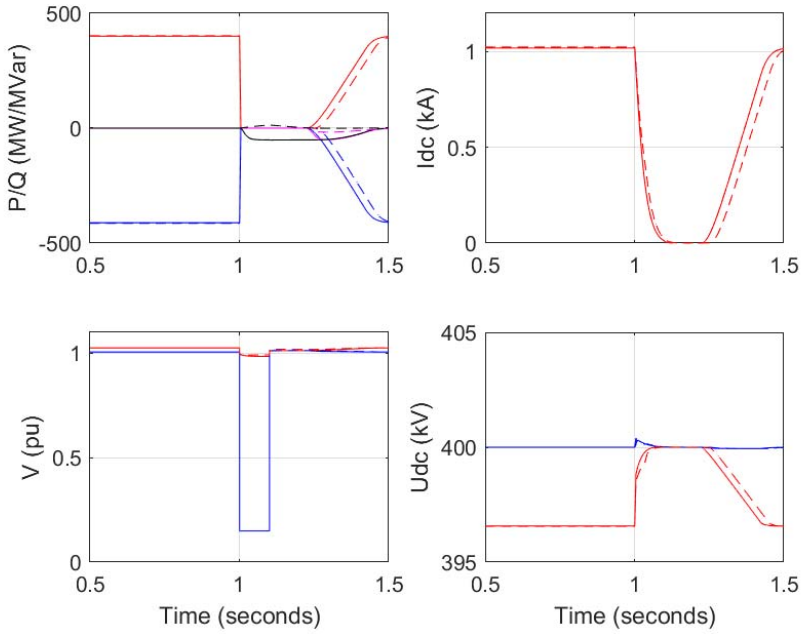

Figure 7: Close-in rectifier side ac fault. **Blue** lines are rectifier quantities. **Red** lines are inverter quantities. **Solid** lines are the user-written vendor specific model. **Dashed** lines are the simple-generic vhvdc1 model, reasonably parameterized, as presented here.

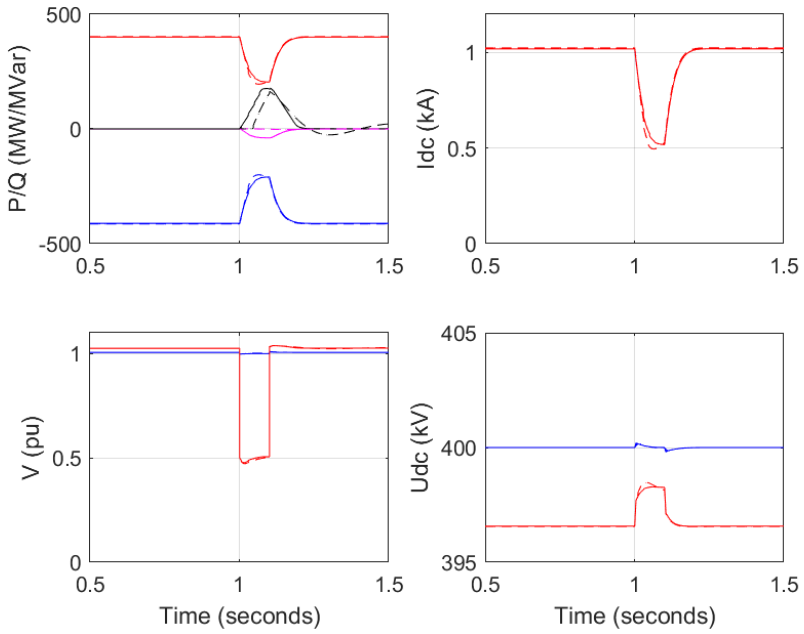

Figure 8: Remote inverter side ac fault. **Blue** lines are rectifier quantities. **Red** lines are inverter quantities. **Solid** lines are the user-written vendor specific model. **Dashed** lines are the simple-generic vhvdc1 model, reasonably parameterized, as presented here.

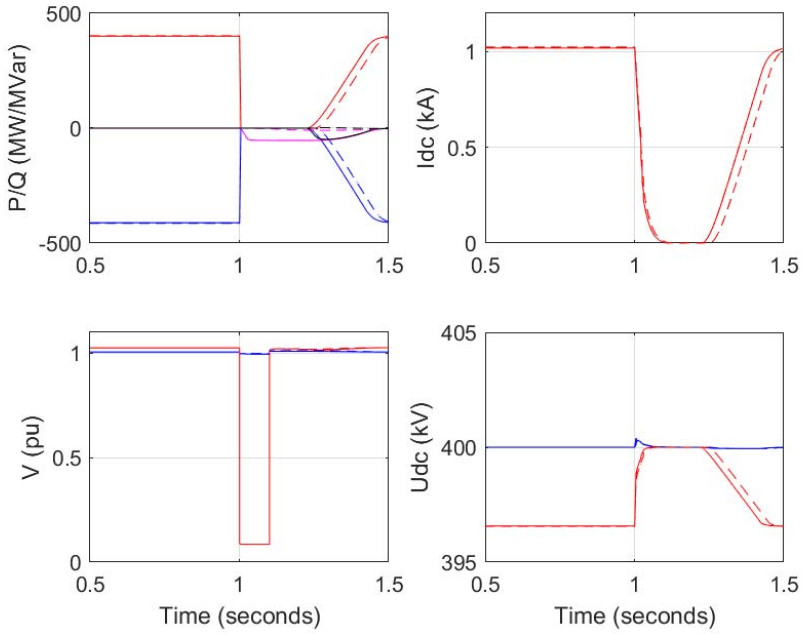

Figure 9: Close-in inverter side ac fault. **Blue** lines are rectifier quantities. **Red** lines are inverter quantities. **Solid** lines are the user-written vendor specific model. **Dashed** lines are the simple-generic vhvdc1 model, reasonably parameterized, as presented here.

2.2 Test Case 2 – Simple Test Case System for Software Benchmarking

A very simple four (bus) system was set-up with an VSC-HVDC in parallel to an ac line, between two large classical generators. The system is shown below in Figure 10.

Figure 10: Simple test system for VSC-HVDC model.

Main Circuit Data:

R = 4 Ω, L =60mH, C = 20 μF

V = 500 Vdc, I = 1000 Adc

MW rating = 500 MW

Power Flow and Dynamics Data:

The power flow solution is shown in Figure 10. The ac line data is as follows (on 100 MVA base):

From	Name	kV	To	Name	kV	CK	ST	R	X	B
2	AC 1 Bus 2	230	1	AC 1 Bus 1	230	1	1	0.0015	0.015	0
3	AC 2 Bus 1	230	4	AC 2 Bus 2	230	1	1	0.002	0.02	0
3	AC 2 Bus 1	230	2	AC 1 Bus 2	230	1	1	0.002	0.02	0

The dynamic model parameters are given in Appendix B. The two classical generators at Bus 1 and 4 are identical and modeled using *gencls*, with the following parameters: MVA = 10000, H = 999999, D= 0, Ra = 0 and X"d = 0.18

The two generators with id "*r*" and "*i*" at bus 2 and 3, respectively, are the rectifier and inverter terminals of the VSC-HVDC. These are not real generators. This is the only way presently to instantiate the model until the model is made part of the software library and the power-flow/dynamics interface established.

Simulations and Results:

The following simulations were executed:

Test 1 – A fault of duration 50 ms, with a fault impedance of X =0.01 pu at bus 1 – rectifier side.

Test 2 – A fault of duration 50 ms, with a fault impedance of X =0.01 pu at bus 4 – inverter side.

Test 3 – A fault of duration 50 ms, with a fault impedance of X =0.001 pu at bus 1 – rectifier side.

Test 4 – A fault of duration 50 ms, with a fault impedance of X =0.001 pu at bus 4 – inverter side.

The results of these simulations are shown below in Figures 11, 12, 13 and 14, respectively.

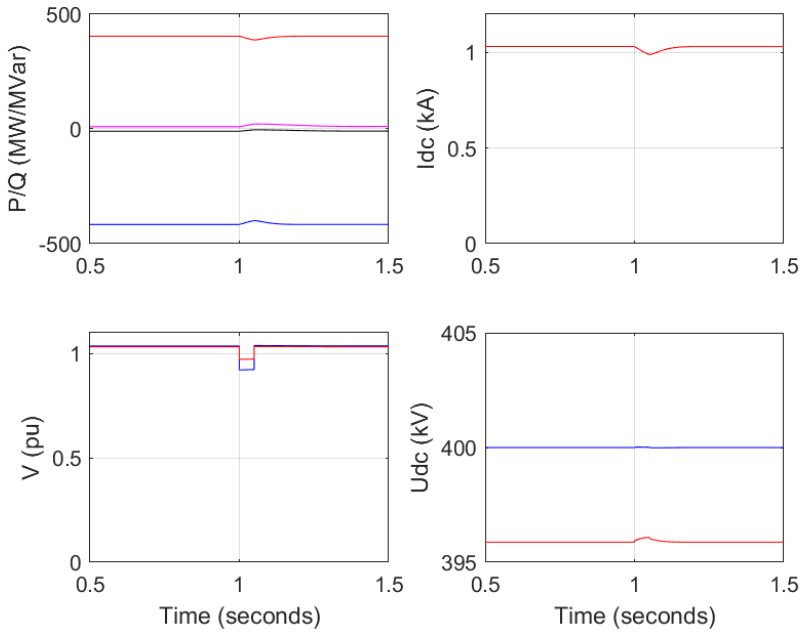

Figure 11: Test 1, remote rectifier side ac fault. **Blue** lines are rectifier quantities. **Red** lines are inverter quantities.

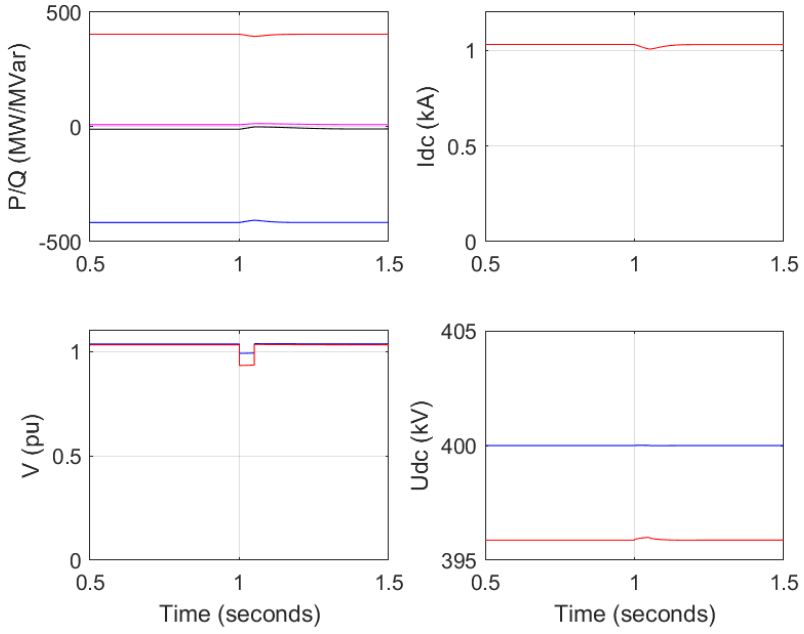

Figure 12: Test 2, remote inverter side ac fault. **Blue** lines are rectifier quantities. **Red** lines are inverter quantities.

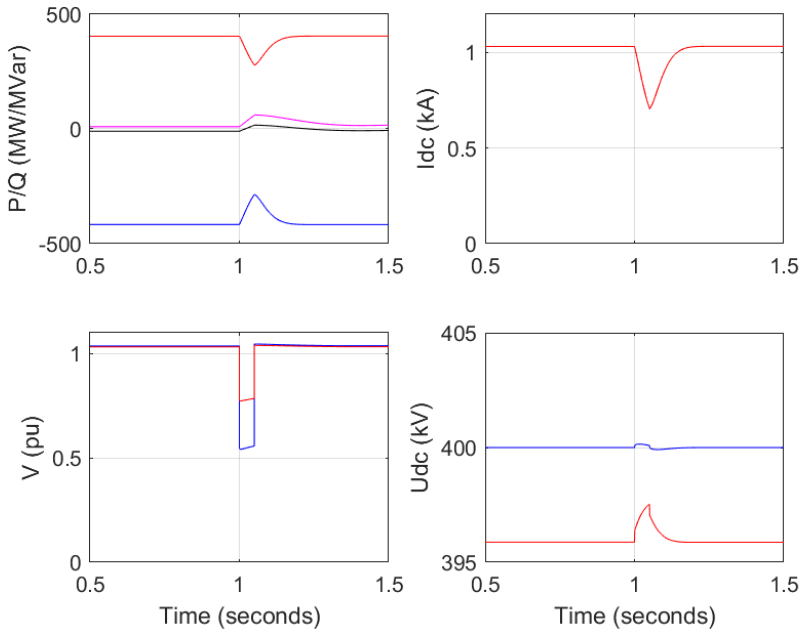

Figure 13: Test 3, close-in rectifier side ac fault. **Blue** lines are rectifier quantities. **Red** lines are inverter quantities.

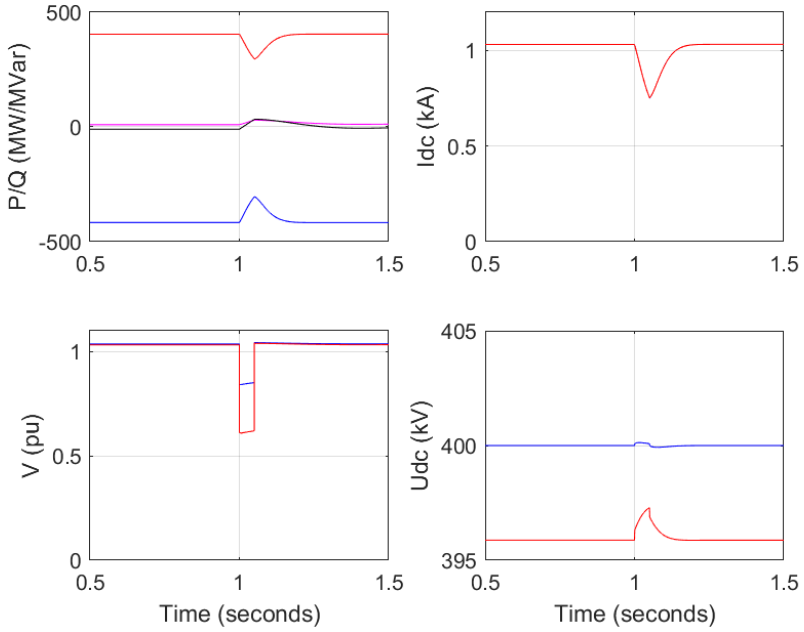

Figure 14: Test 4, close-in inverter side ac fault. **Blue** lines are rectifier quantities. **Red** lines are inverter quantities.

Appendix A: List of Variables, Outputs and Parameters of the vhvdc1 model

A few notes are pertinent:

1. Some internal parameters (e.g. the parameters needed within the model to emulating blocking) are not shown.

2. In this model all dc quantities are in SI units in [kV] and [kA]. Similarly, the power reference Pref and Qac_cmd are in [MW] and [MVar], hence some of the gains etc. below have SI units.

Input Variables

vref_rec – ac voltage reference on the rectifier side (determined by software upon initialization of the model) [pu]

vref_inv – ac voltage reference on the inverter side (determined by software upon initialization of the model) [pu]

pfaref_rec – ac power factor angle reference on the rectifier side (determined by software upon initialization of the model) [rad]

pfaref_inv – ac power factor angle reference on the inverter side (determined by software upon initialization of the model) [rad]

Udref – dc voltage reference; user specified [kV], from power flow

Pref – initial dc power reference, user specified [MW], from power flow

The initial references are all calculated and set by the program upon model initialization from the powerflow solution. These references, thereafter, should be accessible by the user (e.g. through *epcl* in GE PSLF).

Output Variables

Idc_r – dc current rectifier side
Idc_i – dc current inverter side
Udc_r – dc voltage rectifier side
Udc_i – dc voltage rectifier side
Pac_r – ac real power rectifier side
Pac_i – ac real power inverter side
Qac_r – ac reactive power rectifier side
Qac_i – ac reactive power inverter side

Parameters

MW_base	- MW Rating of HVDC	[MW]
Udref	- Initial Rectifier dc Voltage kV	[kV]
Kpi	- proportional gain for dc current control	[kA/kV]

Kii	- integral gain for dc current control	[kA/kV/s]
Kpu	- proportional gain for dc voltage control	[kV/kA]
Kiu	- integral gain for dc voltage control	[kV/kA/s]
Idmax	- maximum dc current reference in kA	[kA]
Idmin	- minimum dc current reference in kA	[kA]
Udmax	- maximum dc voltage reference in kV	[kV]
Udmin	- minimum dc voltage reference in kV	[kV]
Imax	- maximum converter current rating	[pu]
Pmax	- maximum power	[pu]
Pmin	- minimum power	[pu]
eff	- converter efficiency (e.g. 0.99 or 0.98)	[pu]
Rdc	- dc line/cable resistance (ohms)	[ohm]
L	- dc line/cable inductance (mH)	[mH]
C	- dc line/cable capacitance (uF)	[uF]
p1	- points for Pmax - f(Vac)	[pu]
p2	- points for Pmax - f(Vac)	[pu]
p3	- points for Pmax - f(Vac)	[pu]
p4	- points for Pmax - f(Vac)	[pu]
v1	- points for Pmax - f(Vac)	[pu]
v2	- points for Pmax - f(Vac)	[pu]
v3	- points for Pmax - f(Vac)	[pu]
v4	- points for Pmax - f(Vac)	[pu]
v5	- points for Pmax - f(Vac)	[pu]
v6	- points for Pmax - f(Vac)	[pu]
Tr	- Transducer time constant	[s]
vblk_rec	- Voltage below which rectifier blocks	[pu]
vblk_inv	- Voltage below which inverter blocks	[pu]
pll_delay	- Delay in PLL recover after blocking	[s]
unblk	- Voltage above which converter is unblocked	[pu]
Ipmax1	- points on the D-curve vars into the system	[pu]
Ipmax2	- points on the D-curve vars into the system	[pu]
Ipmax3	- points on the D-curve vars into the system	[pu]
Iqmax2	- points on the D-curve vars into the system	[pu]
Iqmax3	- points on the D-curve vars into the system	[pu]
Ipmin1	- points on the D-curve vars from the system	[pu]
Ipmin2	- points on the D-curve vars from the system	[pu]
Ipmin3	- points on the D-curve vars from the system	[pu]
Iqmin2	- points on the D-curve vars from the system	[pu]
Iqmin3	- points on the D-curve vars from the system	[pu]
Tp	- transducer time constant	[s]
Tq	- transducer time constant	[s]
dbd1r	- deadband in voltage control for rectifier	[pu]
dbd1i	- deadband in voltage control for inverter	[pu]
Refflag_r	- 1 voltage control, 0 Q control and 2 pf control	
Refflag_i	- 1 voltage control, 0 Q control and 2 pf control	
Kcr	- Reactive droop rectifier	[pu/MVar]
Kci	- Reactive droop inverter	[pu/MVar]
dbd2r	- deadband in Q control for rectifier	[MVar]
dbd2i	- deadband in Q control for inverter	[MVar]

Kpvr - proportional gain for voltage control rectifier [MVar/pu]
Kivr - integral gain for voltage control rectifier [MVar/pu/s]
Kpqr - proportional gain for Q control for rectifier [MVar/MVar]
Kiqr - integral gain for Q control for rectifier [MVar/MVar/s]
Kpvi - proportional gain for voltage control inverter [MVar/pu]
Kivi - integral gain for voltage control inverter [MVar/pu/s]
Kpqi - proportional gain for Q control for inverter [MVar/MVar]
Kiqi - integral gain for Q control for inverter [MVar/MVar/s]
dQmax - rate of change of Q [MVar/s]
dQmin - rate of change of Q [MVar/s]
dPmax - rate of change of Pref [MW/s]
dPmin - rate of change of Pref [MW/s]
blk_rec - 1 - block, 0 - unblock
blk_inv - 1 - block, 0 - unblock
rec_ublk_stimer - Start unblock timer (logic – 1/0)
inv_ublk_stimer - Start unblock timer (logic – 1/0)
rec_unblk_timer - Unblock timer [s]
inv_unblk_timer - Unblock timer [s]

Appendix B: Parameters for the Simple Test Case in Section 2.2

These parameters here **DO NOT** represent any real project, nor do they profess to be physically meaningful for any project. They are simply some default parameters for the simple test case in section 2.2 for illustrating the performance of the model.

MW_base	500
Udref	500
Kpi	0.05
Kii	50
Kpu	1
Kiu	100
Idmax	1.05
Idmin	0
Udmax	510
Udmin	0
Imax	1.5
Pmax	1.05
Pmin	0
eff	0.99
Rdc	2.5
L	60
C	20
p1	0.5
p2	0.75
p3	0.9
p4	1.01
v1	0.5
v2	0.75
v3	0.9
v4	0.95
v5	1.1
v6	1.3
Tr	0
vblk_rec	0.25
vblk_inv	0.3
pll_delay	0.15
unblk	0.8
Ipmax1	0.9
Ipmax2	0.5
Ipmax3	0.3
Iqmax2	0.5
Iqmax3	0.75
Ipmin1	0.9
Ipmin2	0.5
Ipmin3	0.3
Iqmin2	-0.5
Iqmin3	-0.75
Tp	0.1
Tq	0.1
dbd1r	0
dbd1i	0
Refflag_r	1
Refflag_i	1
Kcr	0
Kci	0
dbd2r	0
dbd2i	0
Kpvr	200
Kivr	500
Kpqr	0
Kiqr	10
Kpvi	200
Kivi	500
Kpqi	0
Kiqi	10
dQmax	99999
dQmin	-99999
dPmax	1000
dPmin	-99999