Proposal for modifications to DER_A

Deepak Ramasubramanian, EPRI
Pouyan Pourbeik, PEACE®
Jens Boemer, EPRI

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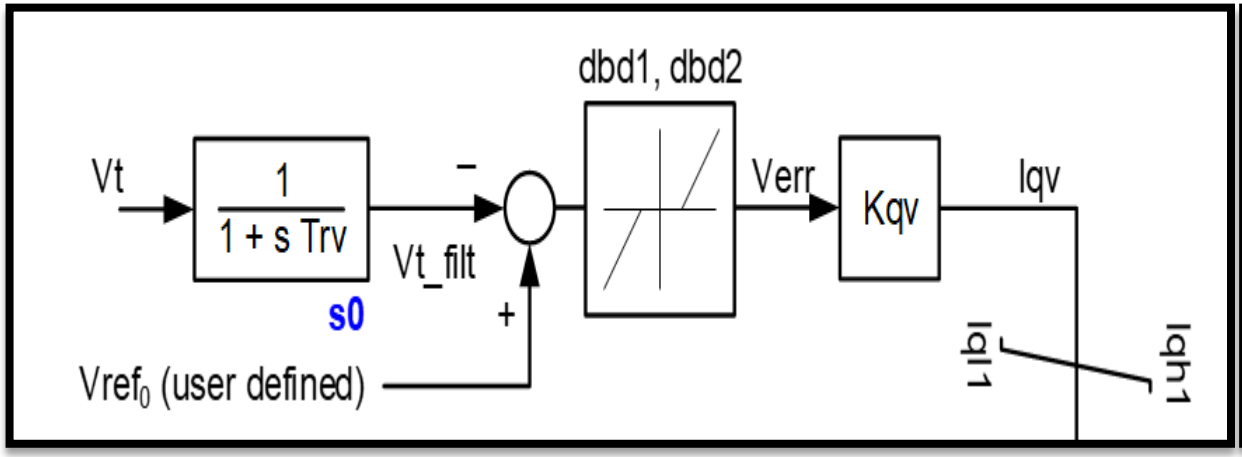
Two proposed modifications

- Dynamic voltage support (DVS) for extended duration of time

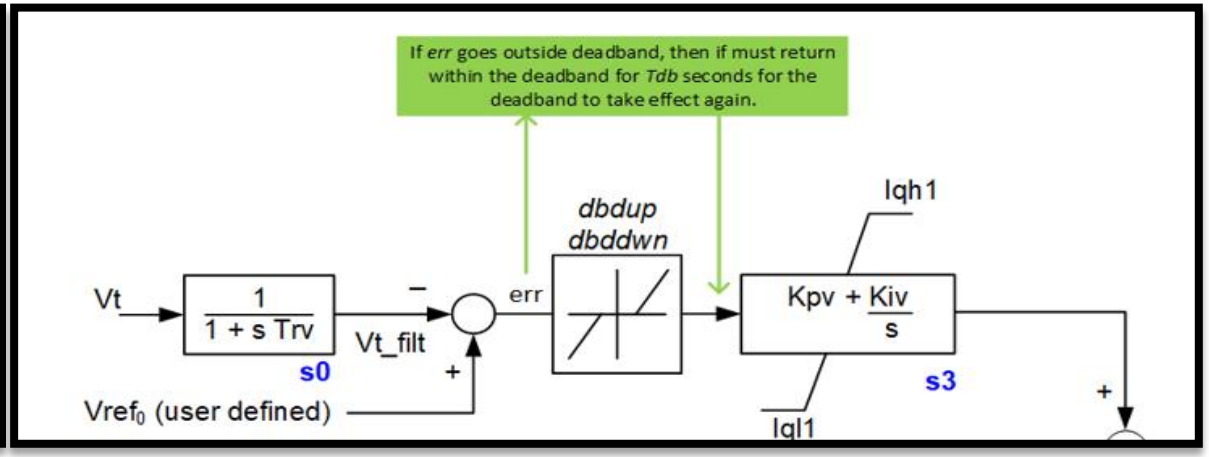
- Additional parallel voltage trip characteristic to represent DER tripping due to unbalanced faults

Dynamic voltage support for extended duration

- Present DER_A model provides dynamic voltage support (DVS) only based on voltage deviation.
- IEEE Std 1547™ – 2018 however allows for the possibility of extended DVS for a user defined amount of time
- Use concept of deadband voltage control loop from SVSMO3 model

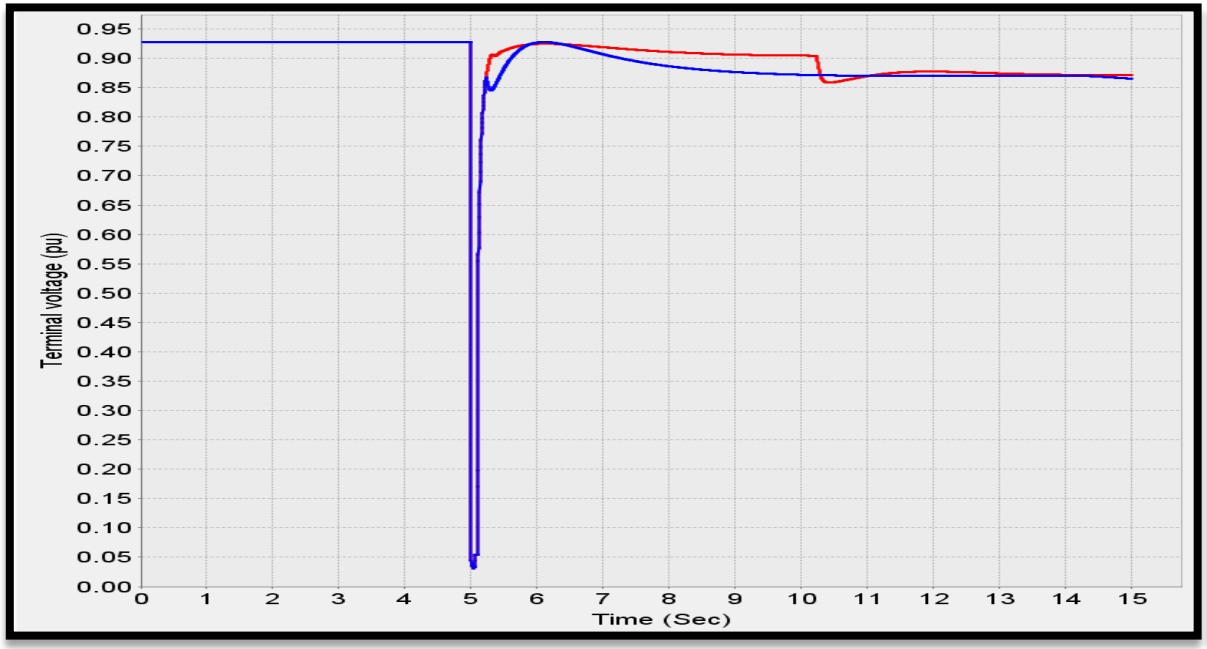


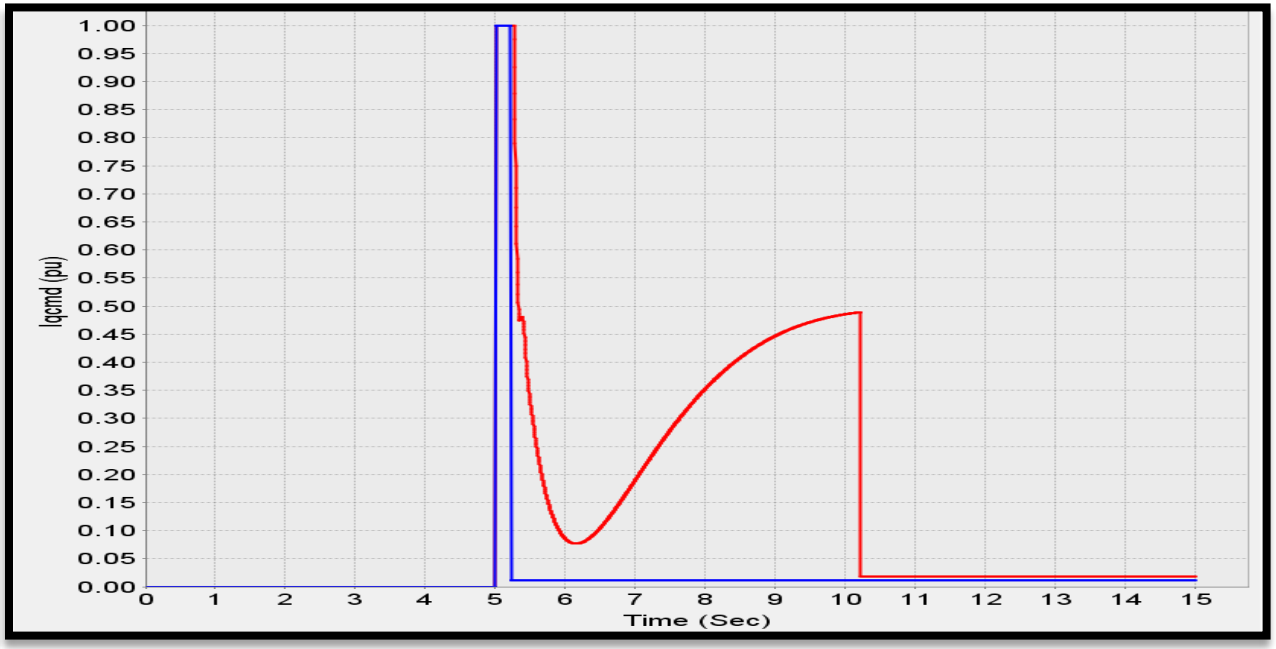
Present DER_A Model



Proposed improvement to DER_A Model

Test case to illustrate model improvement





Blue – Existing DER_A model

Red – Improvement in DER_A model

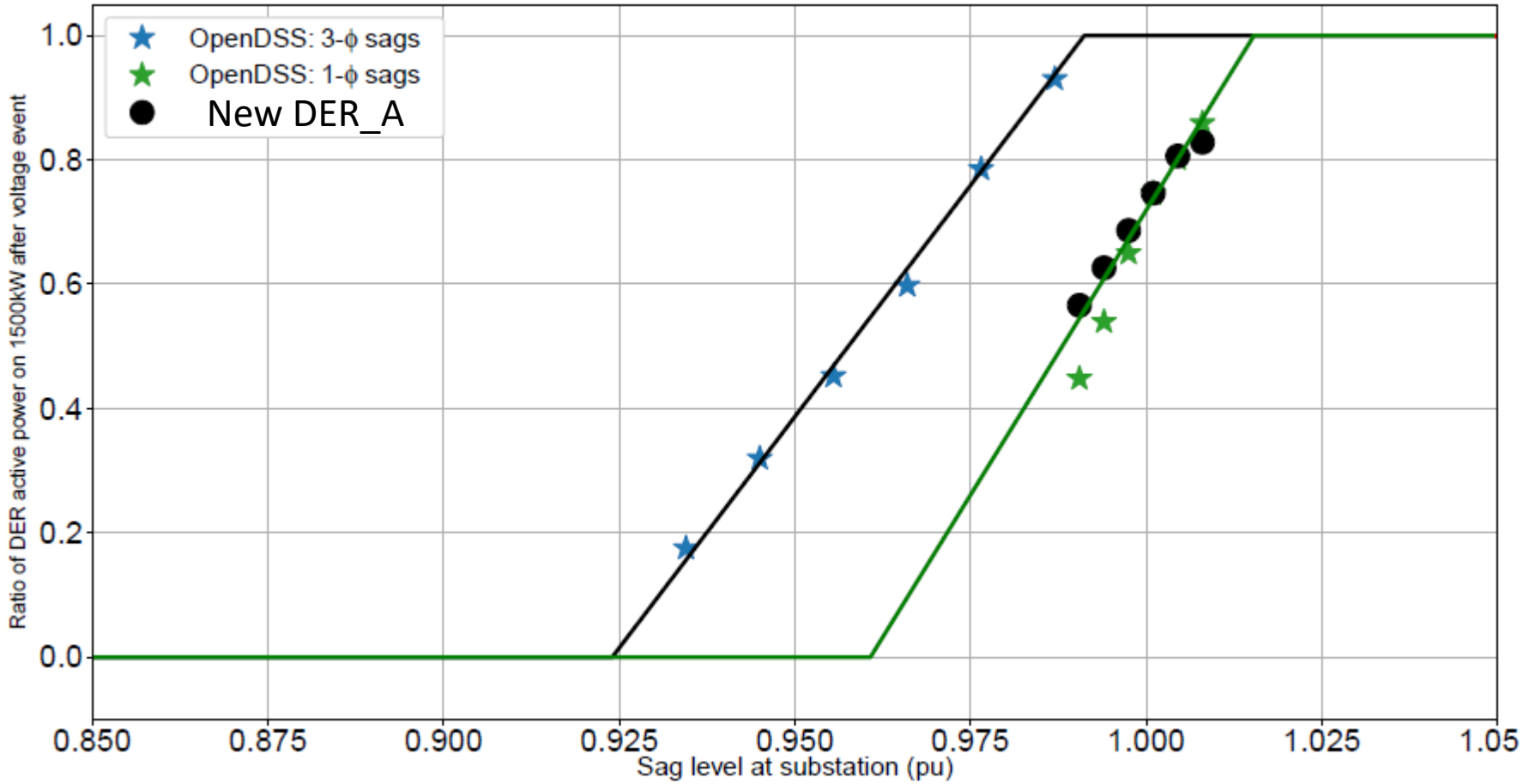
Improvement added to the model is shown to work satisfactorily. Use of this improved feature depends on individual network/case studies/DER interconnections

Parallel voltage trip characteristic for unbalanced faults

- Unbalanced faults cause voltage to reduce only in few phases
- Transformer winding configuration influences the magnitude of distribution voltage dip on all three phases
  - Single phase DER on healthy phase(s) may ride through fault
- Further, positive sequence voltage level due to unbalanced fault is higher than faulted phase voltage
  - For example, for a solid to ground single phase fault on phase A, can result in positive sequence voltage of 0.65pu

Parallel voltage trip characteristic for unbalanced faults

- An additional set of vl1 and vl0 parameters with associated timers
- Simulation program can automatically ‘pick’ this parallel characteristic when unbalanced fault is applied



Yet to be compared against use of PSLF’s sequence voltage meters

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