USER WRITTEN BASIC CONVENTIONAL HVDC MODEL[1]

TO: WECC HVDC TF & EPRI P40.016
FROM: POUYAN POURBEIK, EPRI
SUBJECT: FINAL PROPOSED MODEL SPECIFICATION FOR LCC HVDC
DATE: JANUARY 16, 2015 (REVISED 10/7/15; 10/30/15; 7/1/21[2])
CC:

The current WECC HVDC TF is working on developing simple planning models for both powerflow and dynamic time-domain simulations in positive sequence software tools for HVDC point-to-point transmission. Models are being developed for both conventional line commutated HVDC and voltage source converter (VSC) technology.

The powerflow models for conventional HVDC have always existed in the commercial tools. Recently, the TF completed the definition of the VSC powerflow model and this is being implemented now in the three major North American based tools for official release. Testing was done on beta versions last year.

In terms of dynamic models, the previous memo [1] discussed the proposed models and presented testing, which was subsequently discussed within the HVDC TF and WECC MVWG, and preliminarily approved at the March 2015 MVWG meeting for initial implementation in the commercial tools. At the June MVWG meeting, however, some comments were provided on the *chvdc2* model and it was decided to move forward for now only with that model. Therefore, EPRI hosted a group meeting of the HVDC TF on October 28, 2015[3], where these and other comments were discussed (see minutes of the meeting) and thus the final *chvdc2* model was decided upon, with the intent that the commercial software vendors would subsequently start to implement it (*chvdc2*) and then testing and final approval would be sought in 2016. Thus, this revision of the memo presents the final version of the *chvdc2* model. The *chvdc1* model is also still documented, without change.

Line Commutated HVDC Dynamic Model 1 (*chvdc1*):

The new proposed simple planning model 1 for a line commutated converter (LCC) HVDC is shown below in Figures 1 to 5. This model adopts the high-level control philosophy used in the past by some vendors (e.g. BBC) where the various controls (current, voltage, extinction angle) are effected by separate PI loops and then the final firing angle command selected by a high/low value gate at the rectifier/inverter, respectively.

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[1] Some rather minor typos have been fixed in this very slightly modified version of the original memo. These edits were done on 9/28/17 by P. Pourbeik, PEACE®, based on feedback from J. Senthil, Siemens PTI. Thus, it was not felt necessary to revise the entire memo.

[2] A second round of minor edits were made to fix some typos on 7/1/21; edits made by P. Pourbeik, PEACE®, based on feedback from Michał Kosmecki, Instytut Energetyki Oddział Gdańsk and J. Senthil, Siemens PTI.

[3] Present at the meeting were: Dave Dickmander, ABB; Eric Heredia, BPA; Pouyan Pourbeik, EPRI; Bill Price, GE; Juan Sanchez-Gasca, GE; Jay Senthil, Siemens PIT; Jamie Weber, PowerWorld

Line Commutated HVDC Dynamic Model 2 (*chvdc2*):

The new proposed simple planning model 2 for an LCC-HVDC is shown below in Figures 6 to 7. This model adopts the high-level control philosophy used by vendors such as ABB, where a since PI loop controls the firing angle and the other control objectives are achieved by dynamically controlling the main PI loop controller limits. Note that for this case the Voltage Dependent Current Order Limit (VDCOL) model remains the same as that shown in Figure 3 and 4.

The list of model parameters for both models is provided in the Appendix A.

In this revised memo several changes have been made to *chvdc2*, based on the collected group decisions at the TF meeting on 10/28/15. These changes are:

1. The optional AC VDCOL was changed such that it can be switched on or off as shown in Figure 8 (see [4] for a description of its use in PDCI). The DC VDCOL is always effective. These two functions, if used together, must be properly coordinated. The AC VDCOL option was only added to the *chvdc2* user-written model, but in the final library implementation of the two models by the commercial vendors, if so decided by WECC, it can easily be added to both models. IMPORTANT NOTE: *Tvd* cannot be zero or negative; the user must be warned and prevented from entering a value that is inappropriate (i.e. zero or negative). Also, if upon initialization Vacr and/or Vaci are less than Vac_ref, then this is not a reasonable state. The user must be warned to correct the value of Vac_ref, and or one can in the code force Vac_ref to a value equal to the minimum of Vacr/Vaci.

2. At the request of ABB, a rectifier alpha minimum limiter (RAML) was added to the rectifier controls as shown in Figure 6. This is a simple emulation that reasonable capture the behavior of the RAML function, it is not an exact representation of actual equipment controls.

3. In the Appendix C the collective decision on how to model commutation failure at the inverter and also how to model the DC line dynamics is described. These two features have not been modeled or tested here, because they need to be implemented in the actual core c-code of GE PSLF™ (and core of other tools). Currently the line dynamics is modeled internally in the *dcmt* or *dc2t* models to which the *epcl* code presented here interfaces. Therefore, in the final library implementation of *chvdc2*, the line dynamics (as described in Appendix C) and commutation failure emulation, will need to be incorporated into for example *dc2t* and then combined with the controls implemented here in *epcl* to constitute *chvdc2*. The model invocation will then require the user to define the ac commutating bus of the rectifier and inverter, respectively, together with all the parameters associated with *chvdc2*.

4. The following parameters were removed:

    a. *Vdiv* – make this a hardcoded value of 0.05 and not a parameter (see Figure 7)

    b. *r_comp_r* and *r_comp_i* were removed (i.e. dc voltage is feed directly into the VDCOL without any current compensation, i.e. *r_comp* × *Idc* component).

Test Case:

A simple benchmark test case system, based on the CIGRE benchmark case [2], was established for testing these models. The results and data is provided below in the Appendix B.

For simplicity, in none of these cases have we emulated commutation failure. Also, none of the simulations apply the AC VDCOL function for these initial tests.

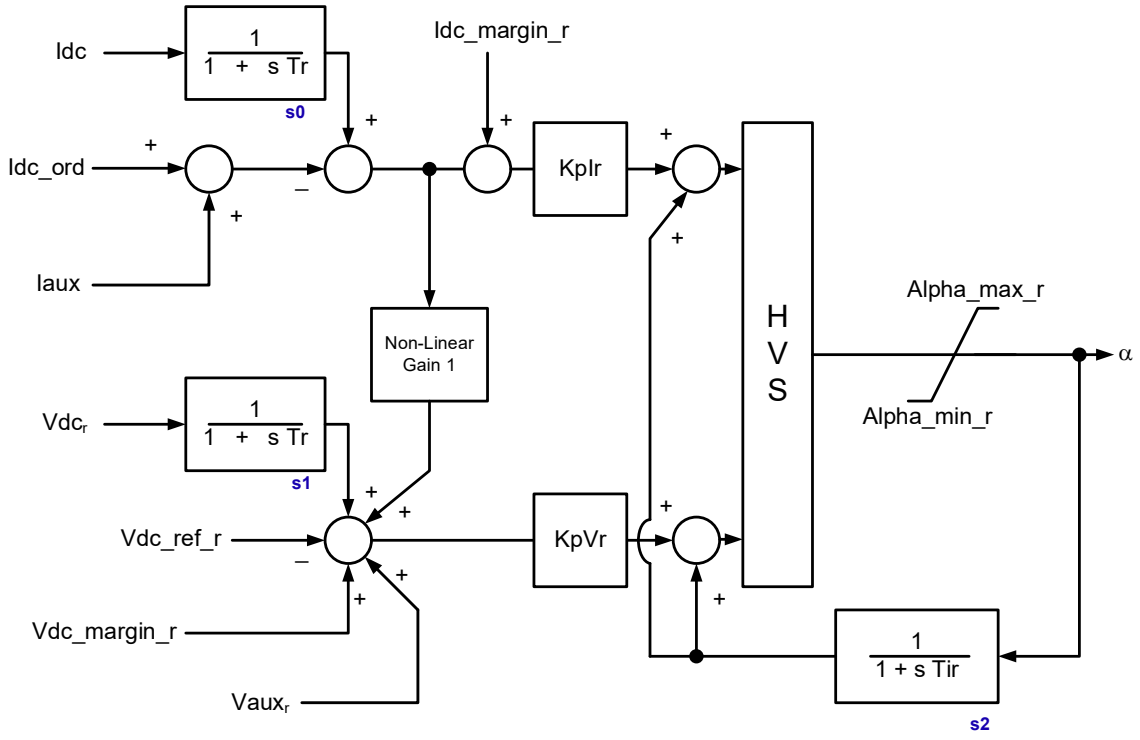


Figure 1: Rectifier controls

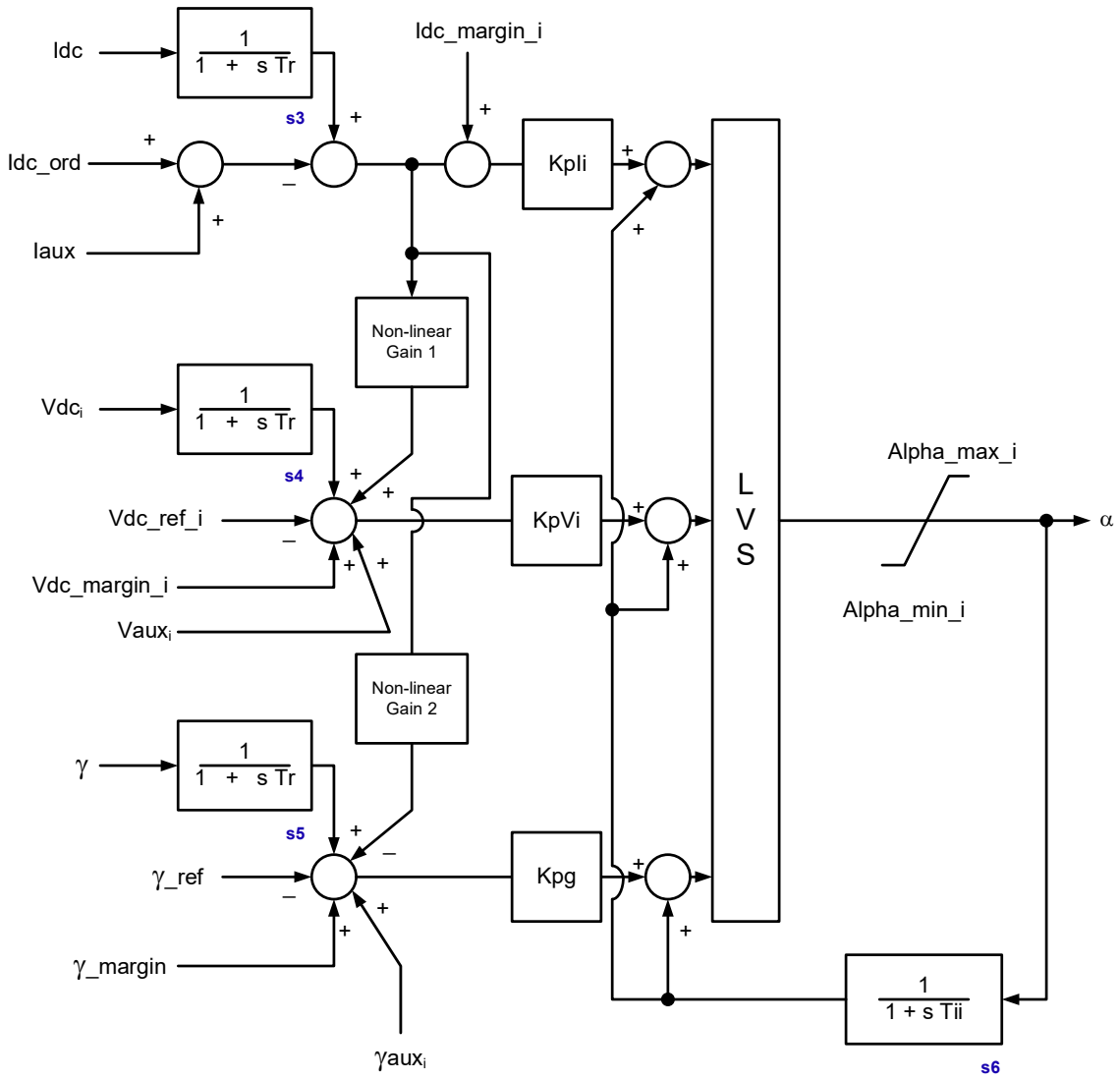


Figure 2: Inverter Controls

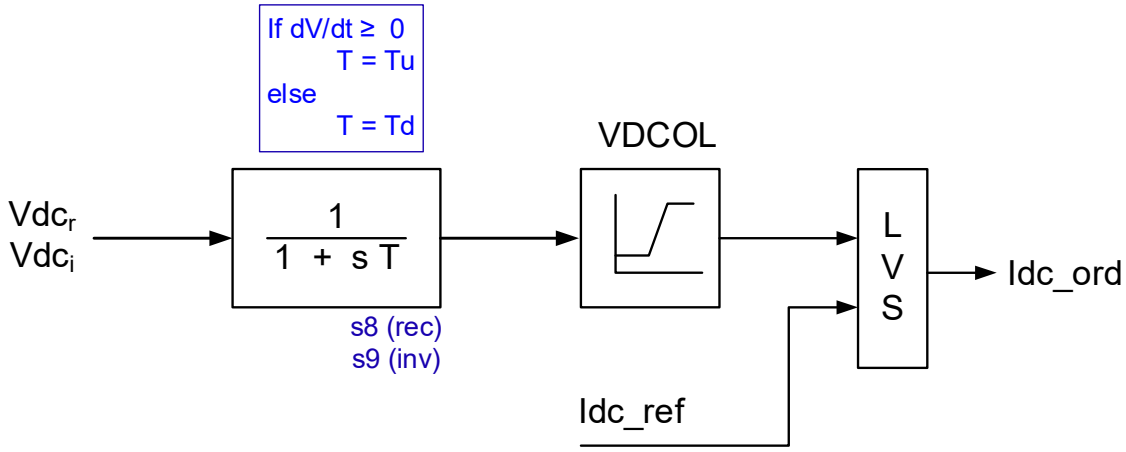


Figure 3: VDCOL control logic

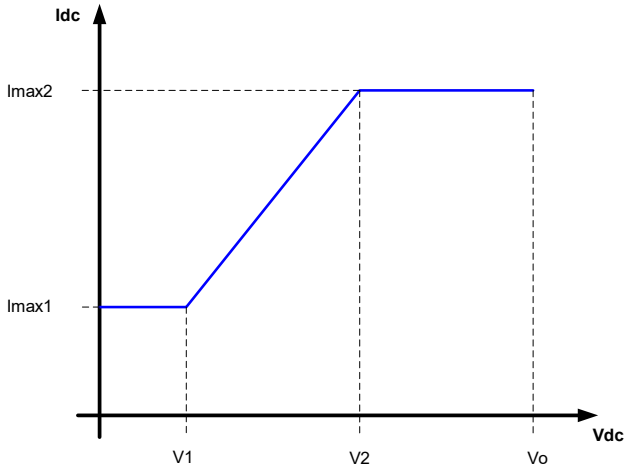


Figure 4: VDCOL lookup table.

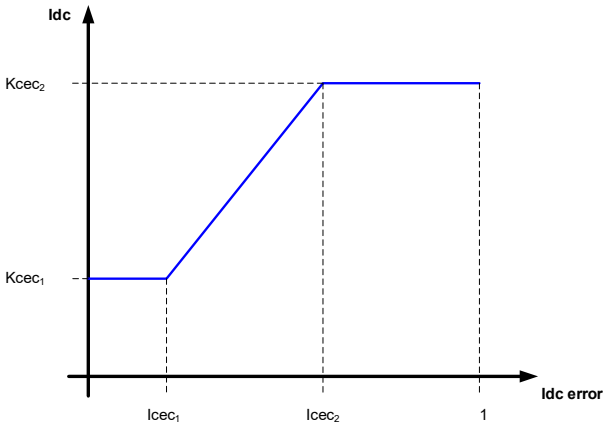


Figure 5: Non-linear Gain lookup table.

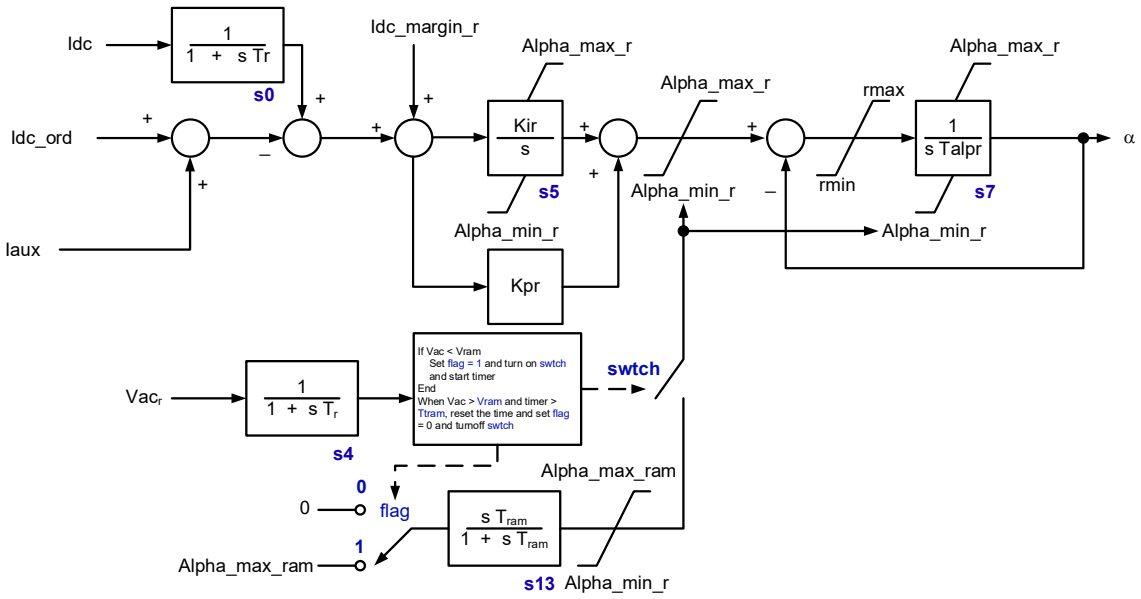


Figure 6: Rectifier controls for *chvdc2* model.

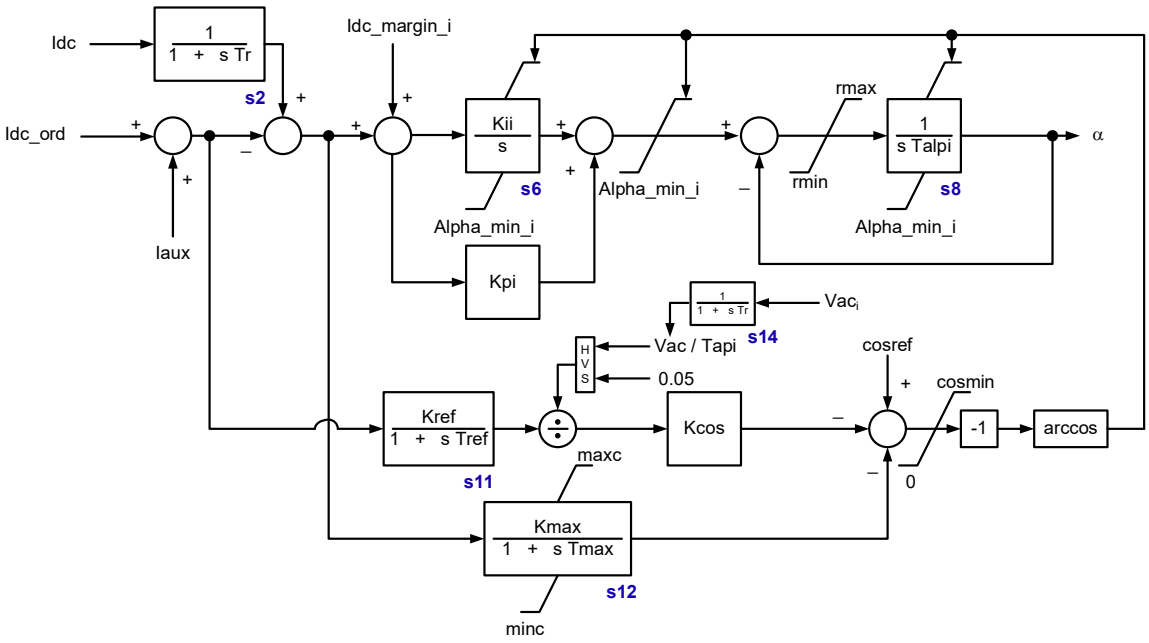


Figure 7: Inverter controls for *chvdc2* model.

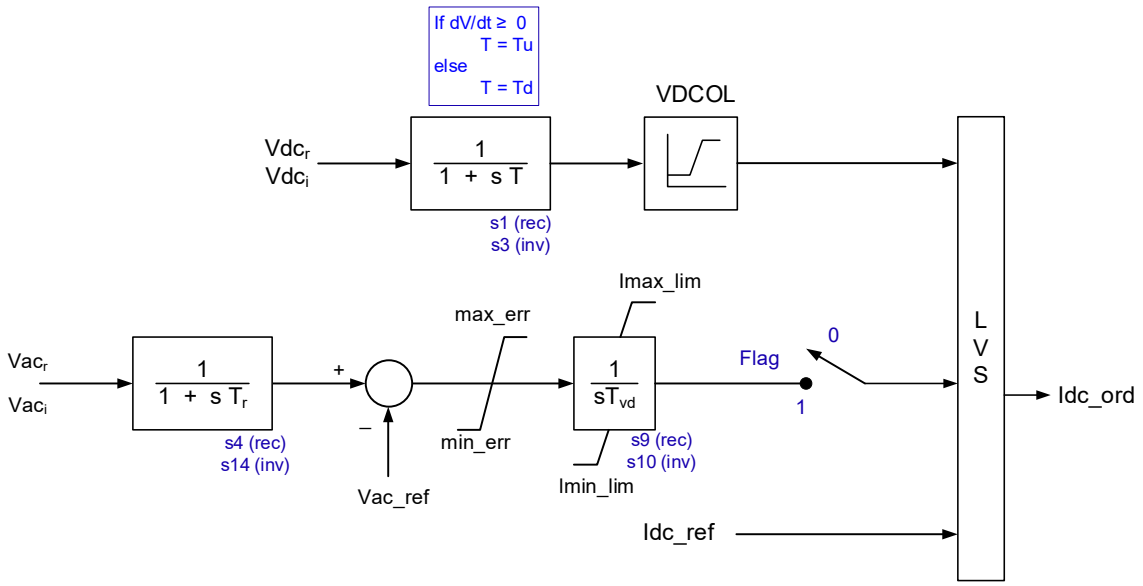


Figure 8: The DC VDCOL is always effective, while by setting Flag to either 0 or 1 the optional and additional AC voltage dependent current order limit can be disabled or activated, respectively. It is important to understand the usage of the AC VDCOL and that it must be properly coordinated with the DC VDCOL (see [4]).

Appendix A: Parameter List for Models

Parameter/Variable List for chvdc1:

Input Variables

Idc	– dc current
Idc_ord	– dc current order as determined from the VDCOL
Vdc_r	– dc voltage rectifier side
Vdc_i	– dc voltage inverter side
γ	– gamma (extinction angle)
Vdc_ref_r	– initial dc voltage reference on rectifier side
Vdc_ref_i	– initial dc voltage reference on inverter side
γ_ref	– initial gamma reference
Iaux	– auxiliary input to dc current control added on rectifier and inverter side (typically unused = 0)
$Vaux_r$	– auxiliary input to dc voltage control on rectifier side (typically unused = 0)
$Vaux_i$	– auxiliary input to dc voltage control on inverter side (typically unused = 0)
γaux_i	– auxiliary input to gamma control on inverter side (typically unused = 0)

The auxiliary inputs are provided for additional flexibility, in case a user-written or supplemental model is to be connected to this model for specific applications. All these auxiliary inputs should be accessible by the user (e.g. through *epcl* in GE PSLF™). **Note:** Iaux must go to both the rectifier and inverter side, since there can only be one current order given to both converter stations.

The initial references are all calculated and set by the program upon model initialization from the powerflow solution. These references, thereafter, should be accessible by the user (e.g. through *epcl* in GE PSLF™).

The dc current and voltages are determined at each integration time step by the dc network model and are variables of the converter equations. Likewise for gamma.

Output Variables

α_r	– rectifier firing angle
α_i	– inverter firing angle
γ	– inverter extinction angle
Idc_r	– dc current rectifier side
Idc_i	– dc current inverter side
Vdc_r	– dc voltage rectifier side
Vdc_i	– dc voltage rectifier side
Pac_r	– ac real power rectifier side
Pac_i	– ac real power inverter side
Qac_r	– ac reactive power rectifier side
Qac_i	– ac reactive power inverter side

Parameters

KpIr	– proportional gain for current control for rectifier controls
KpVr	– proportional gain for voltage control for rectifier controls

Alpha_max_r – maximum alpha on rectifier side
Alpha_min_r – minimum alpha on rectifier side
Idc_margin_r – dc current margin on rectifier side
Vdc_margin_r – dc voltage margin on rectifier side
Tr – measurement transducer time constant
rcomp_r – compensating resistance rectifier side in ohms
Kcecr_1 – non-linear gain rectifier side
Kcecr_2 – non-linear gain rectifier side
Icecr_1 – non-linear gain rectifier side
Icecr_2 – non-linear gain rectifier side

KpIi – proportional gain for current control for inverter controls
KpVi – proportional gain for voltage control for inverter controls
Kpg – proportional gain for gamma control for inverter controls
Tii – inverter alpha control time constant
Apha_max_i – maximum alpha on inverter side
Alpha_min_i – minimum alpha on inverter side
Idc_margin_i – dc current margin on inverter side
Vdc_margin_i – dc voltage margin on inverter side
γ_margin – gamma margin on inverter side
γ_ref – gamma reference
rcomp_i – compensating resistance inverter side in ohms
Kceci_1 – non-linear gain 1 inverter side
Kceci_2 – non-linear gain 1 inverter side
Iceci_1 – non-linear gain 1 inverter side
Iceci_2 – non-linear gain 1 inverter side
Kceci_3 – non-linear gain 2 inverter side
Kceci_4 – non-linear gain 2 inverter side
Iceci_3 – non-linear gain 2 inverter side
Iceci_4 – non-linear gain 2 inverter side

Imax1 – VDCOL break point 1
Imax2 – VDCOL break point 2
V1 – VDCOL break point 1
V2 – VDCOL break point 2
Tur – VDCOL Measurement transducer time constant for voltage rising rectifier side
Tdr – VDCOL Measurement transducer time constant for voltage falling rectifier side
Tui – VDCOL Measurement transducer time constant for voltage rising inverter side
Tdi – VDCOL Measurement transducer time constant for voltage falling inverter side

L_{line} – DC line inductance (mH)
L_{smr_rec} – The inductance of the smoothing reactor at the rectifier end (mH)
L_{smr_inv} – The inductance of the smoothing reactor at the inverter end (mH)
C – DC line capacitance (μF)

gamma_cf – angle below which commutation failure is likely (default value = 10^{o})

Tcf – minimum time duration that commutation failure is likely to last (default value = 0.034 seconds)
Vac_ucf – voltage above which converter will recover from commutation failure (default value = 0.9)

Parameter/Variable List for chvdc2:

Input Variables
Idc – dc current
Idc_ord – dc current order as determined from the VDCOL
Iaux – auxiliary input to dc current control on rectifier and inverter side (typically unused = 0)
cosref – initial reference for limit control
Tapi – total tap ratio of the converter transformer calculated from the powerflow data

The auxiliary inputs are provided for additional flexibility, in case a user-written or supplemental model is to be connected to this model for specific applications. All these auxiliary inputs should be accessible by the user (e.g. through *epcl* in GE PSLF™). **Note:** Iaux must go to both the rectifier and inverter side, since there can only be one current order given to both converter stations.

The initial reference, *cosref*, is calculated by the program upon model initialization from the powerflow solution. It is set such that the firing angle controls on the inverter side initializes on its upper limit (i.e. alpha_max_i on the inverter side = initial alpha on the inverter side). This reference, thereafter, should be accessible by the user (e.g. through *epcl* in GE PSLF™).

The dc current and voltages are determined at each integration time step by the dc network model and are variables of the converter equations.

Output Variables

α_r – rectifier firing angle
α_i – inverter firing angle
γ – inverter extinction angle
Idc_r – dc current rectifier side
Idc_i – dc current inverter side
Vdc_r – dc voltage rectifier side
Vdc_i – dc cvoltage rectifier side
Pac_r – ac real power rectifier side
Pac_i – ac real power inverter side
Qac_r – ac reactive power rectifier side
Qac_i – ac reactive power inverter side

Parameters

Talpr – time constant for current control for rectifier controls
Kir – integral gain for current control for rectifier controls
Kpr – proportional gain for current control for rectifier controls
Alpha_max_r – maximum alpha on rectifier side

Alpha_min_r – minimum alpha on rectifier side
Idc_margin_r – dc current margin on rectifier side
maxc – constant
minc – constant
rmax – constant
rmin – constant
Tr – measurement transducer time constant
Talpi – time constant for current control for inverter controls
Kii – integral gain for current control for inverter controls
Kpi – proportional gain for current control for inverter controls
Kcos – proportional gain for alpha max calculation loop
Kref – gain for alpha max calculation loop on Iref
Tref – time constant for alpha max calculation loop on Iref
Kmax – proportional gain for alpha max calculation loop on Ierr
Tmax – time constant for alpha max calculation loop on Ierr
cosmin_i – constant
Alpha_min_i – minimum alpha on inverter side
Idc_margin_i – dc current margin on inverter side

Imax1 – VDCOL break point 1
Imax2 – VDCOL break point 2
V1 – VDCOL break point 1
V2 – VDCOL break point 2
Tur – VDCOL Measurement transducer time constant for voltage rising rectifier side
Tdr – VDCOL Measurement transducer time constant for voltage falling rectifier side
Tui – VDCOL Measurement transducer time constant for voltage rising inverter side
Tdi – VDCOL Measurement transducer time constant for voltage falling inverter side

Flag – If = 1 then use AC VDCOL is in-service, else it is dsiabled
Imax_lim – VDCOL output current order maximum limit
Imin_lim – VDCOL output current order minimum limit
max_err – VDCOL AC voltage input error maximum limit
min_err – VDCOL AC voltage input error minimum limit
Tvd – VDCOL integrator time constant
Vac_ref – VDCOL AC voltage reference (pu)

alpha_max_ram – Rectifier Alpha Min Limiter (RAML) max alpha
Tram – RAML washout time constant
Vram – RAML ac voltage setpoint
Ttram – RAML timer

L_{line} – DC line inductance (mH)
L_{smr_rec} – The inductance of the smoothing reactor at the rectifier end (mH)
L_{smr_inv} – The inductance of the smoothing reactor at the inverter end (mH)
C – DC line capacitance (μF)

gamma_cf – angle below which commutation failure is likely (default value = 10^{o})

Tcf – minimum time duration that commutation failure is likely to last (default value = 0.034 seconds)

Vac_ucf – voltage above which converter will recover from commutation failure (default value = 0.9)

Appendix B: Tests Case and Results

This first test case is a simple system with two equivalent areas and a point-to-point conventional line-commutated HVDC. This test system is depicted in Figure A-1 below.

Using the test case developed in [2] as a starting point, below is the data for this test case. It should be noted that there are some significant differences between the test case proposed in [1] and what is presented here for several reasons:

1. The test case in [2] was primarily developed for use in electromagnetic transient (EMT) type programs and so has main circuit data (e.g. specific filter bank elements) which are not relevant to power flow and stability modeling (e.g. the filter banks are represented here as a fixed, lumped shunt capacitor, neglecting filter inductive and resistive elements).

2. The test case in [2] is based on a 50 Hz system, whereas the one here is a 60 Hz equivalent.

3. Some aspects of the model in [2] are not specified or pertinent to establishing a useful power flow and stability simulation set (e.g. MVA rating and parameters for equivalent generators for the two AC systems) and so these have been defined here using reasonable, assumed, values.

4. Some parameters were changed to result in a more simple and reasonable power flow solution for the test case used here (e.g. lumped capacitors used in [2] to emulate line charging are neglected, and some of the line parameters were rounded off etc.).

5. The power flow direction in our case here is reversed compared to [2]. This is not particularly of much importance or consequence, but should be noted (i.e. in the test case here the inverter is on the 345 kV side).

IMPORTANT DISCLAIMER:

As noted in [8] the model presented in that document is neither a representation of any actual HVDC system, nor necessarily a typical main-circuit design. This is equally true of the test case(s) presented here. The test case(s) presented here are only for the purpose of testing the proposed HVDC models and should not be viewed in any other context.

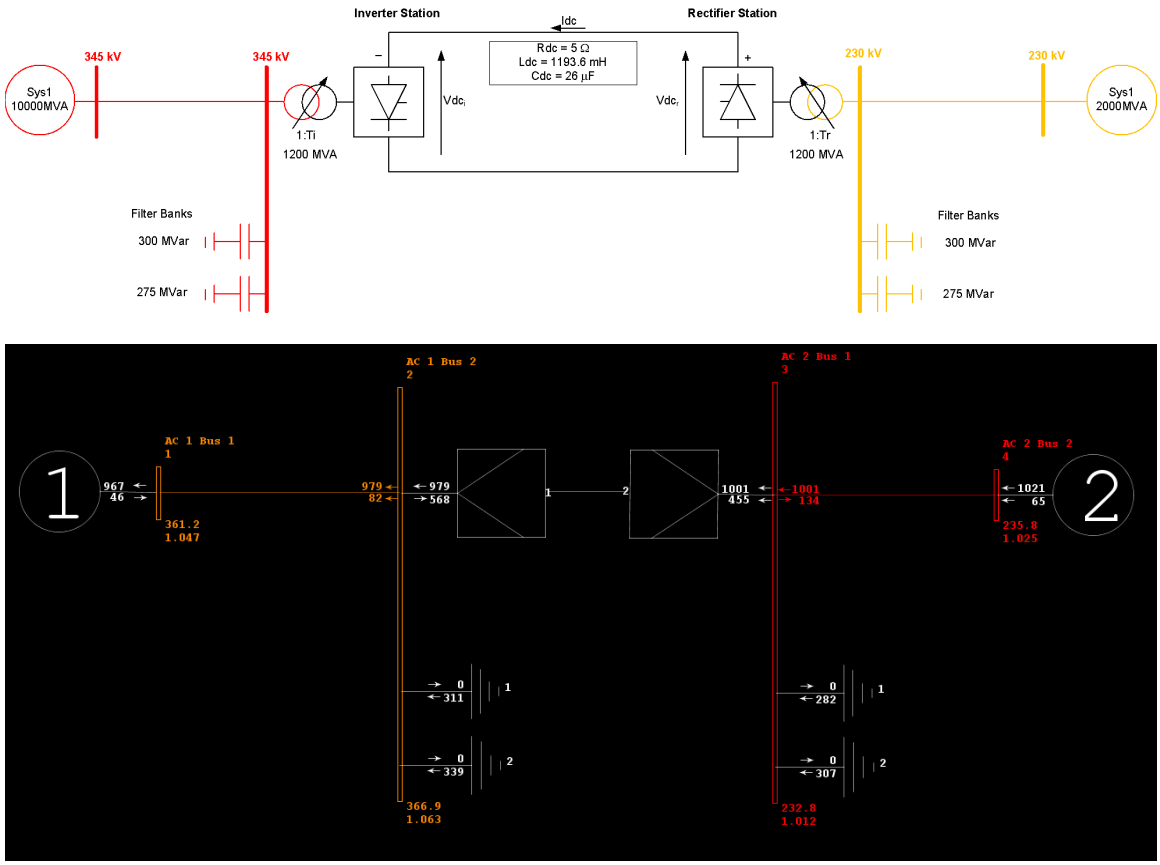


Figure A-1: Simple CIGRE benchmark case.

Main Circuit Data

R = 5 Ω, L = 1193 mH, C = 26 µF
V = 500 Vdc, I = 2000 A

Simulation Results

Two faults were simulated [3]:

1. A 3-phase fault at bus 4 (rectifier side system) for 50 ms and a fault impedance of 0.005 pu on system MVA base.
2. A 3-phase fault at bus 1 (inverter side system) for 50 ms and a fault impedance of 0.005 pu on system MVA base.

Rectifier Side Fault:

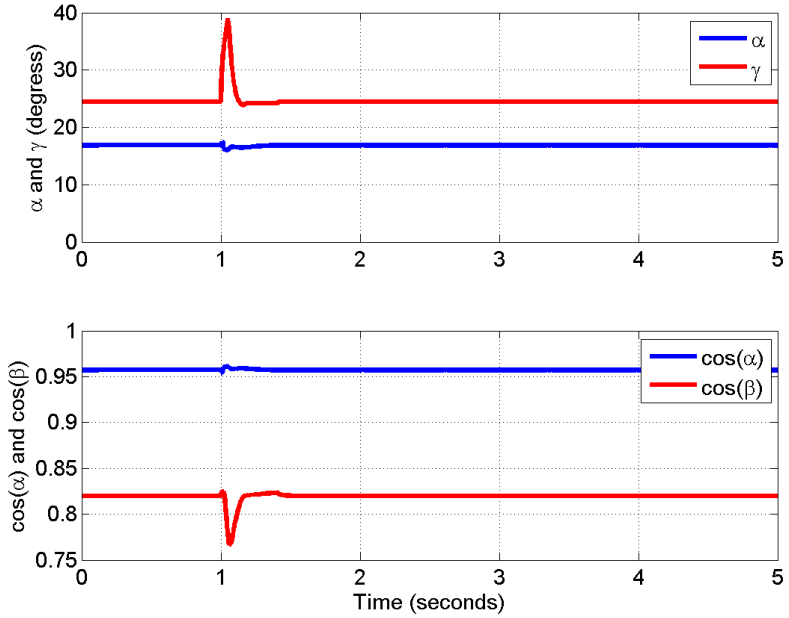


Figure B-1: Angles and cosine of firing angle; chvdc1, rectifier side ac fault.

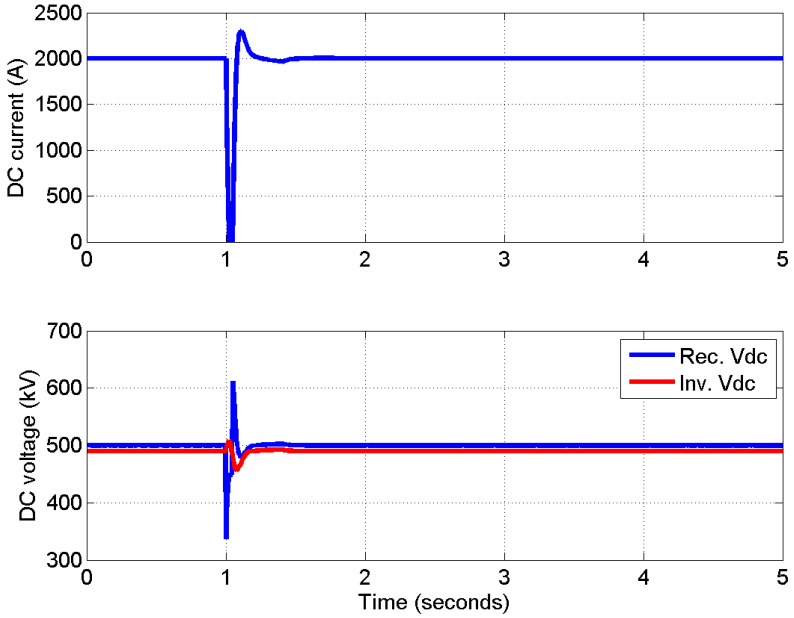


Figure B-2: DC current and voltage; chvdc1, rectifier side ac fault.

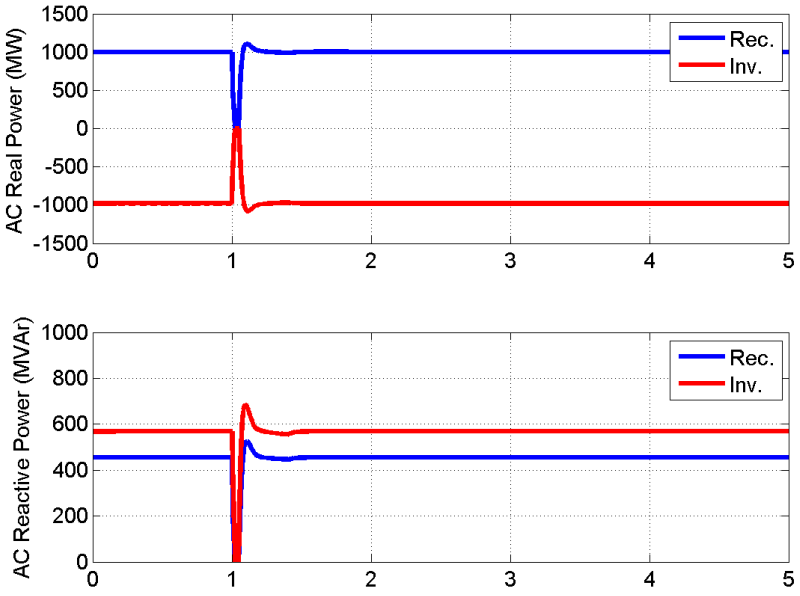


Figure B-3: Real and reactive AC power; chvdc1, rectifier side ac fault.

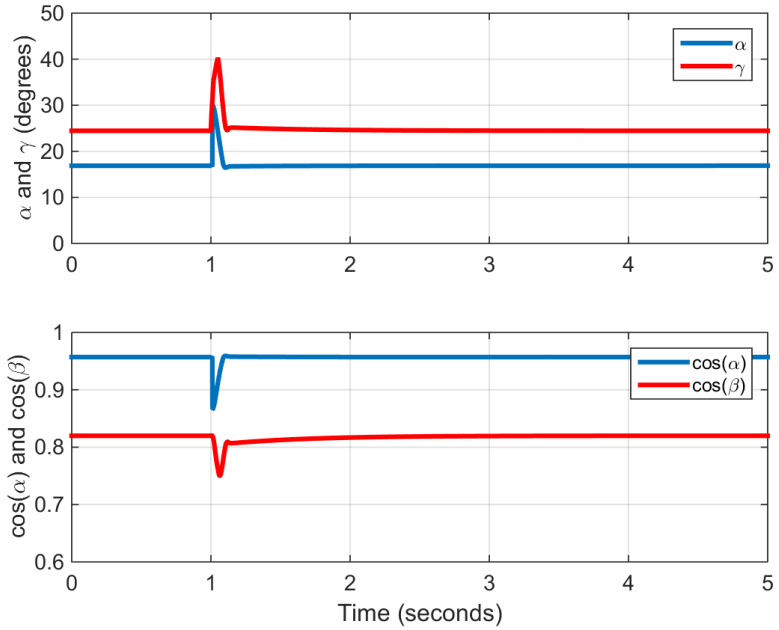


Figure B-4: Angles and cosine of firing angle; chvdc2, rectifier side ac fault.

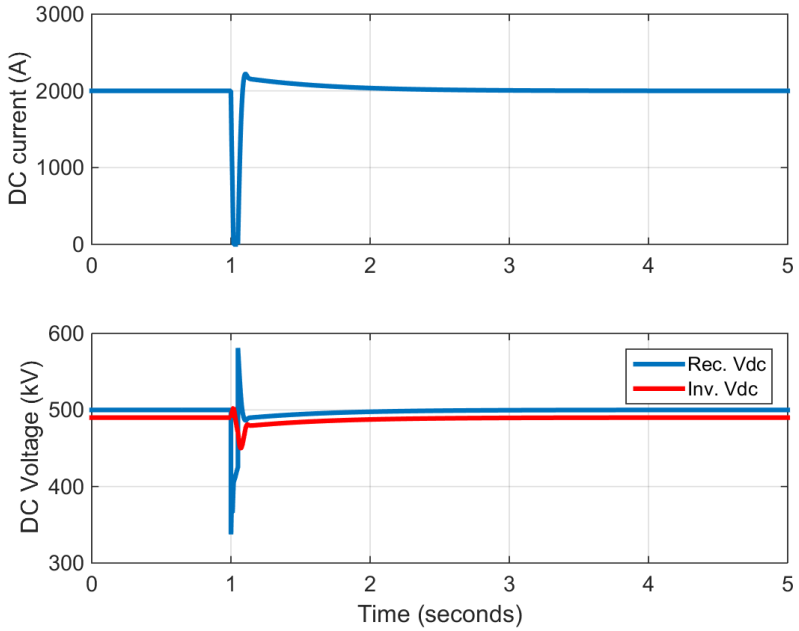


Figure B-5: DC current and voltage; chvdc2, rectifier side ac fault.

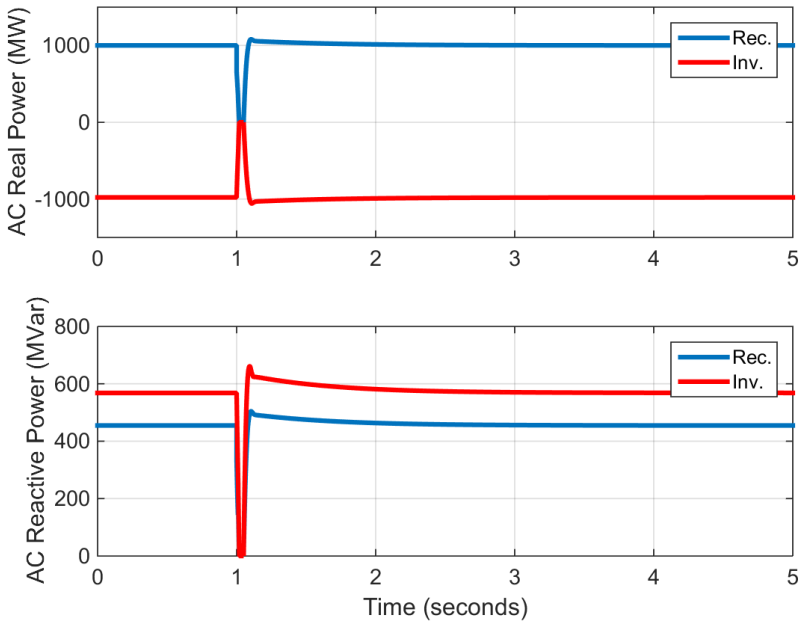


Figure B-6: Real and reactive AC power; chvdc2, rectifier side ac fault.

Inverter Side Fault:

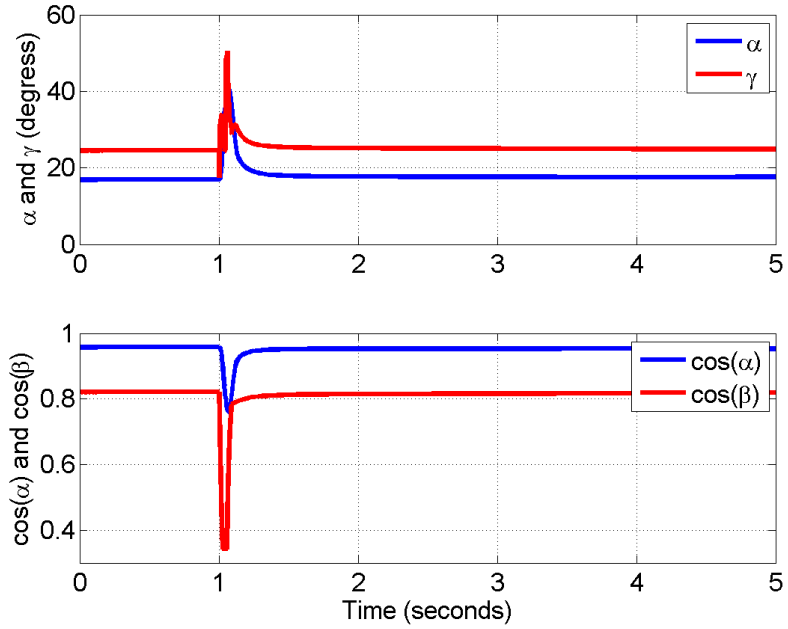


Figure B-8: Angles and cosine of firing angle; chvdc1, inverter side ac fault.

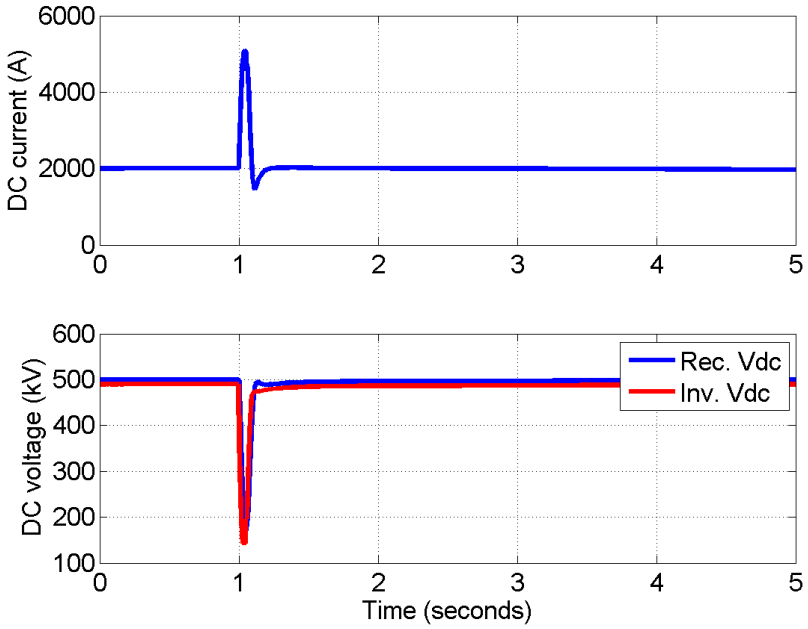


Figure B-9: DC current and voltage; chvdc1, inverter side ac fault.

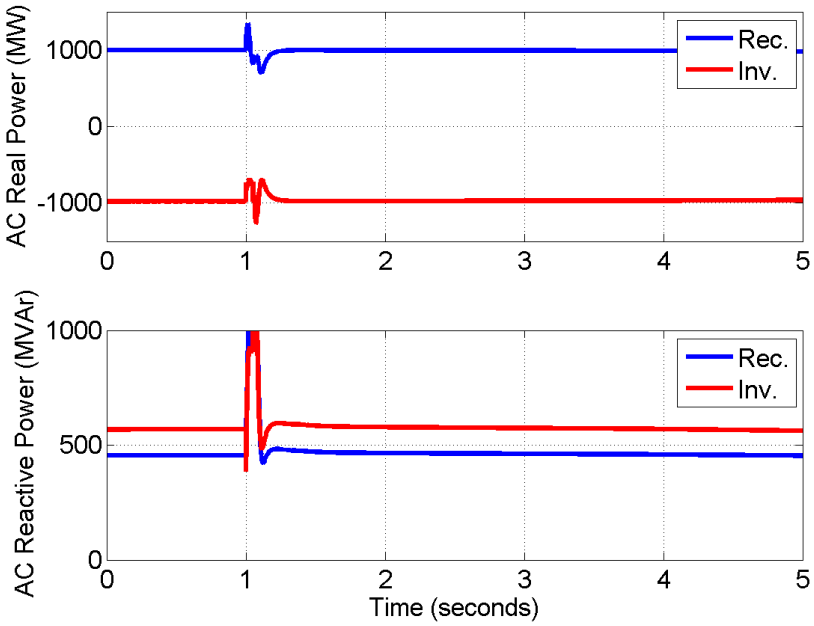


Figure B-10: Real and reactive AC power; chvdc1, inverter side ac fault.

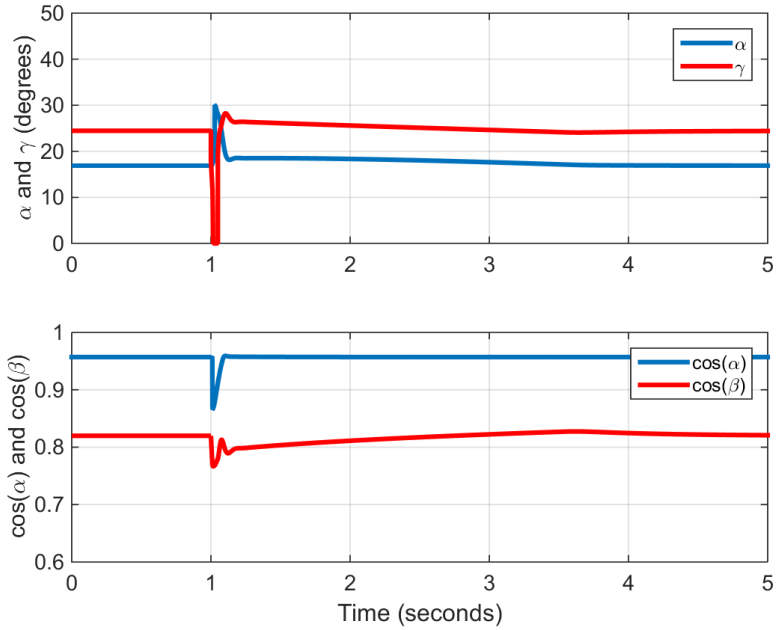


Figure B-11: Angles and cosine of firing angle; chvdc2, inverter side ac fault.

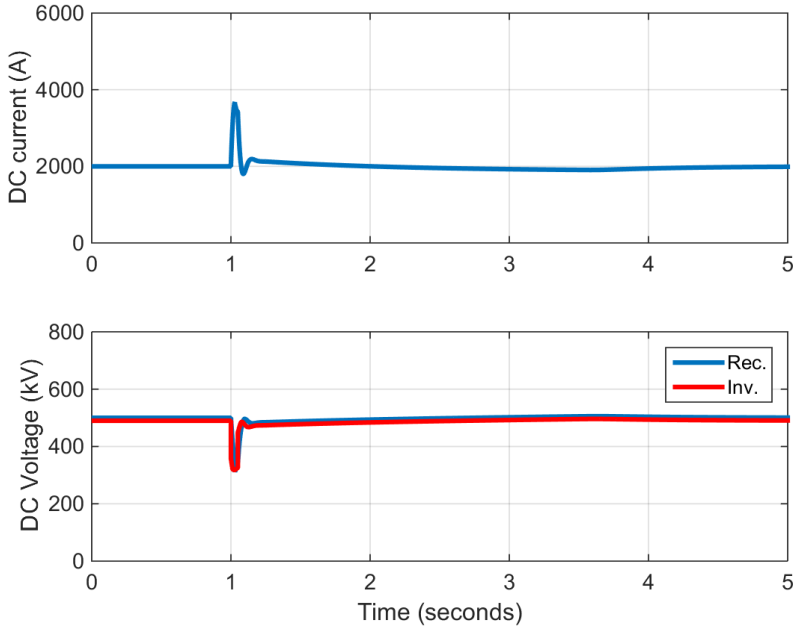


Figure B-12: DC current and voltage; chvdc2, inverter side ac fault.

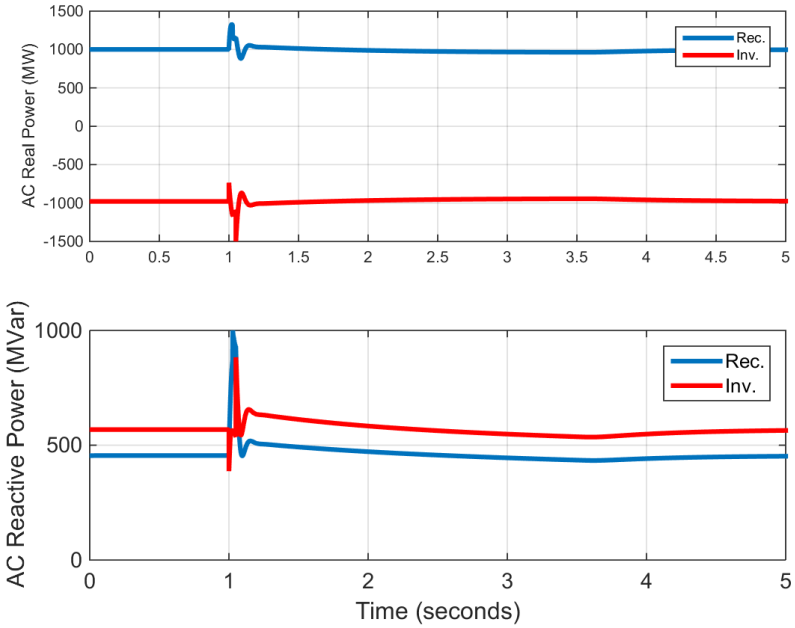


Figure B-13: Real and reactive AC power; chvdc2, inverter side ac fault.

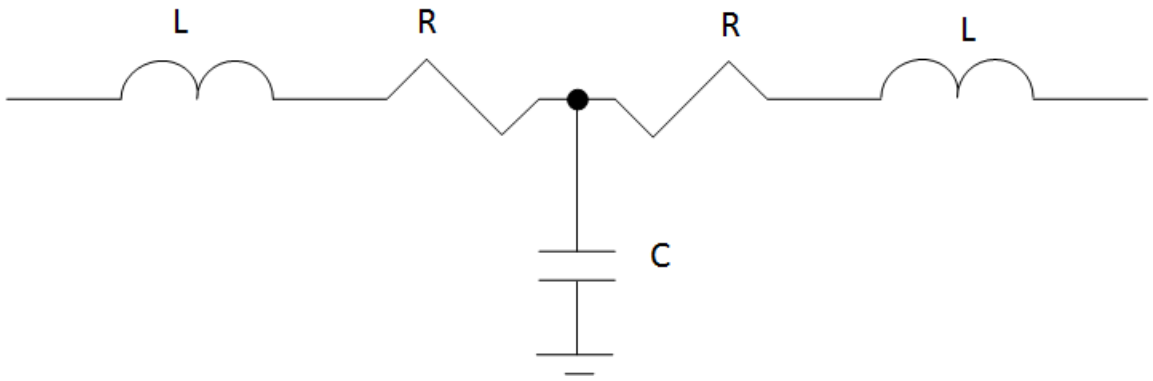
Appendix C: DC Line Modeling and Emulation of Commutation Failure

At the 10/28/15 HVDC TF meeting the following items were agreed upon. Those present were:

Dave Dickmander, ABB
Eric Heredia, BPA
Pouyan Pourbeik, EPRI
Bill Price, GE
Juan Sanchez-Gasca, GE
Jay Senthil, Siemens PTI
Jamie Weber, PowerWorld

DC Line modeling:

The DC line model will be as follows:



where

L = (total effective line or cable inductance)/2
R = (total line or cable resistance)/2
C = total line or cable capacitance

and

total effective line or cable inductance[4] = L_{line} + (L_{smr_rec} + L_{smr_inv}) + Nbr×1.75×(L_{com_rec} + L_{com_inv})

where the inductances are as explained below in the parameter list and Nbr is the number of 6-pulse bridges (typically, this would be set to 2 since most HVDC systems are 12-pulse).

[4] The 1.75 factor is an approximation of the time-average value of commutating inductance due to overlap. See CIGRE-92 "DC Side Harmonics and Filtering in HVDC Transmission Systems" or M. P. Bahrman, K. J. Peterson and R. H. Lasseter, "DC system resonance analysis", IEEE Trans. PWRD, January 1987.

To solve the DC line equations an inner integration loop will be used inside the dc model with an integration step equal to (h/n), where h is the integration time step of the main simulation and n is an integer. The integer n is calculated $n \geq 3.f_n.h$, i.e. the first integer greater than $3.f_n.h$. For example, if f_n = 500 Hz and h = ¼ cycle (0.00416 s), then n = 7. Also, fn is the natural resonant frequency of the above circuit = $\frac{1}{2\pi\sqrt{LC}}$; the program should give the user a warning if the frequency is too high (i.e. n > 10) and indicate that the L and C in the model has been neglected in this case and the user should choose other values.

Parameters:

L_{line} , L_{smr_rec}, L_{smr_inv} and C are, respectively, the line inductance, smoothing reactor inductance on the rectifier and inverter side, and line capacitance and should be parameters of the dynamic model

R, L_{com_rec}, L_{com_inv} (or X_{com_rec} and X_{com_inv}) are, respectively, the line resistance and rectifier/inverter commutating inductance (reactance) and should be parameters if the power flow converter models

Commutation Failure:

It was agreed that the following approximate method would be used to emulated commutation failure, internal to the model. It must be realized that this is a "rough" compromise. The actual dynamics and characteristics of commutation failure can only truly be modeled and studied in 3-phase EMT type simulations of the actual equipment.

Three additional parameters are needed in the dynamic modes:

gamma_cf – angle below which commutation failure is likely (default value = 10^o)
Tcf – minimum time duration that commutation failure is likely to last (default value = 0.034 seconds)
Vac_ucf – voltage above which converter will recover from commutation failure (default value = 0.9)

Thus, the logic for emulating commutation failure will be as follows:

state = normal

If $\gamma \leq$ gamma_cf

- short inverter (i.e. set DC voltage = 0; but DC current still flows)
- state = comm_fail
- start timer (Timer)

end

If state = comm_fail

If (Timer ≥ Tcf) and (Vac_comm_bus ≥ Vac_ucf)

- state = normal
- release the short circuit on the inverter model
- reset timer (Timer)

end

end

Keep executing the above code at every time step and network solution to make sure commutation failure is invoked and removed promptly as necessary.

Checks on data entry:

1. If the user sets gamma_cf = 0, then the model will not emulate commutation failure at all.
2. If the user sets a value for gamma_cf that is higher than gamma_min (entered in the converter power flow model), then the dynamic model should printer an error message warring the user of this issue and disable this feature (i.e. set gamma_cf = 0)
3. If the user enters a value of Vac_ucf ≥ 0.95, the model should print a warring message indicating to the user that a suspect value is being used and this is more typically 0.9 pu or less.
4. If the user enters a value of Tcf ≥ 0.05, the model should print a warring message indicating to the user that a suspect value is being used and this is more typically 0.03 to 0.05 seconds or less.

References:

[1] P. Pourbeik, "Implementation and testing of the conventional HVDC model", dated 10/27/14; issued to WECC HVDC Task Force and EPRI P40.016. (revised 10/7/15)

[2] M. Szechtman, T. Wess, C. V. Thio, H. Ring, L. Pilotto, P. Kuffel and K. Mayer, "First Benchmark Model for HVDC Control Studies", CIGRE Report of WG 14.02, Electra Magazine, 1991.

[3] *Technical Update on HVDC Modeling*, EPRI, Palo Alto, CA: 2014. Product ID 3002003348.

[4] R. Bunch and D. Kosterev, "Design and Implementation of AC Voltage Dependent Current Order Limiter at Pacific HVDC Intertie", IEEE Trans. PWRD, January 2000.