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Memorandum

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TO: WECC REMTF

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SUBJECT: **TEST PROTOCOL FOR BENCHMARKING OF DER_A MODEL WITHIN CMPLDW MODEL ACROSS SOFTWARE PLATFORMS**

This document describes the proposed test protocol for benchmarking the working of the composite load model with the presence of the DER_A model across multiple software platforms for use in positive sequence time domain simulations.

Figure 1 shows the test system setup that will be used for the benchmarking process while Table 1 tabulates the network details.

Figure 1Benchmark test system

Table 1Details of the network

From Bus	From Bus Name	To Bus	To Bus Name	R (pu)	X (pu)	Charging B (pu)
1	BUS1 69.000	2	BUS2 69.000	0.0025	0.01	0

The source at Bus 1 will be modeled as a play-in voltage source. The load at Bus 2 will consist of 30 MW of constant power load (to be represented by the CMPLDW model) and 10 MW of DER (to be represented by the DER_A model)

In this round of benchmark testing, the load will always be set at a non-zero value. It is expected that the validation of the code transfer for inclusion of the DER_A model within the composite load model has already been carried out in each software platform along the lines of [1].

Table 2 tabulates the various tests that will be performed in this round of testing the model. Detailed description of some of the tests are provided after the table

Table 2 List of various tests to be performed

Test number		**Description**	
Test 1	A	Play-in a voltage sag immediately followed by a voltage swell. This voltage waveform would cause partial voltage trip to occur in DER_A	Load composition being only Motor A and with DER_A
	B		Load composition being only Motor B and with DER_A
	C		Load composition being only Motor C and with DER_A
	D		Load composition being only Motor D and with DER_A
Test 2	A	Play-in a voltage waveform which would cause trip and reconnection of Motor A	Load composition being only Motor A and with DER_A
	B	Play-in a voltage waveform which would cause stall and restart of Motor D	Load composition being only Motor D and with DER_A

Test 3		Play-in an under frequency waveform	Load composition being 50% Motor A, 50% Motor D, and DER_A
Test 4	A	With load composition being 10% Motor A, 10% Motor B, 5% Motor C, 40% Motor D, 15% static load, 20% power electronic load, and with DER_A, apply a 0.1s fault on Bus 2 with fault X = 0.005pu	Load = 30 MW, DER = 1 MW
	B		Load = 30 MW, DER = 10 MW
	C		Load = 30 MW, DER = 30 MW
	D		Load = 30 MW, DER = 45 MW
	E		Load = 1 MW, DER = 75 MW
	F	Same fault conditions as above, but reactance between bus 1 and bus 2 increased to 0.5pu	Load = 1 MW, DER = 75 MW

Test Number 1

The play-in waveform for this test is as shown in Figure 2. A voltage sag of 0.7pu is applied at 1.0s for a duration of 15 cycles on 60 Hz. Immediately after that, the voltage is raised to 1.2pu for another 15 cycles of 60 Hz. The recovery level after the high voltage event is 1.05pu with a ramp time of 1.0s for the voltage to come back to 1.0pu.

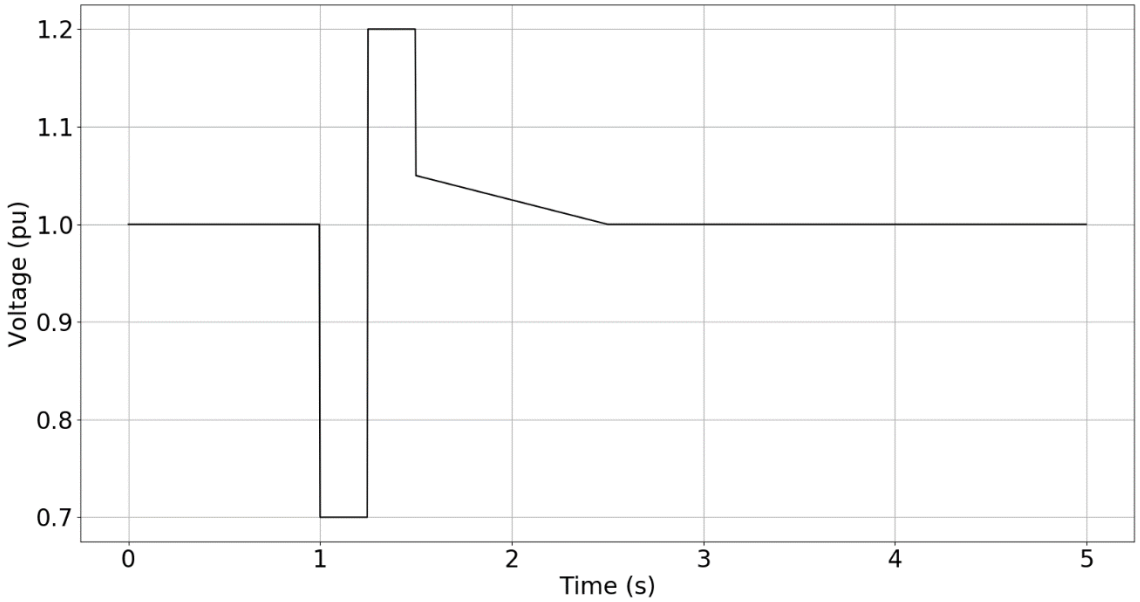

Figure 2 Play-in voltage waveform for Test 1

Test Number 2A

The play-in waveform for this test is as shown in Figure 3. At 1s, the voltage is reduced from 1 pu to 0.4 pu over 0.5s, held at 0.4 pu for 5 cycles at 60 Hz, and ramped back to 1 pu in 0.5s. The simulation is run for till 5s

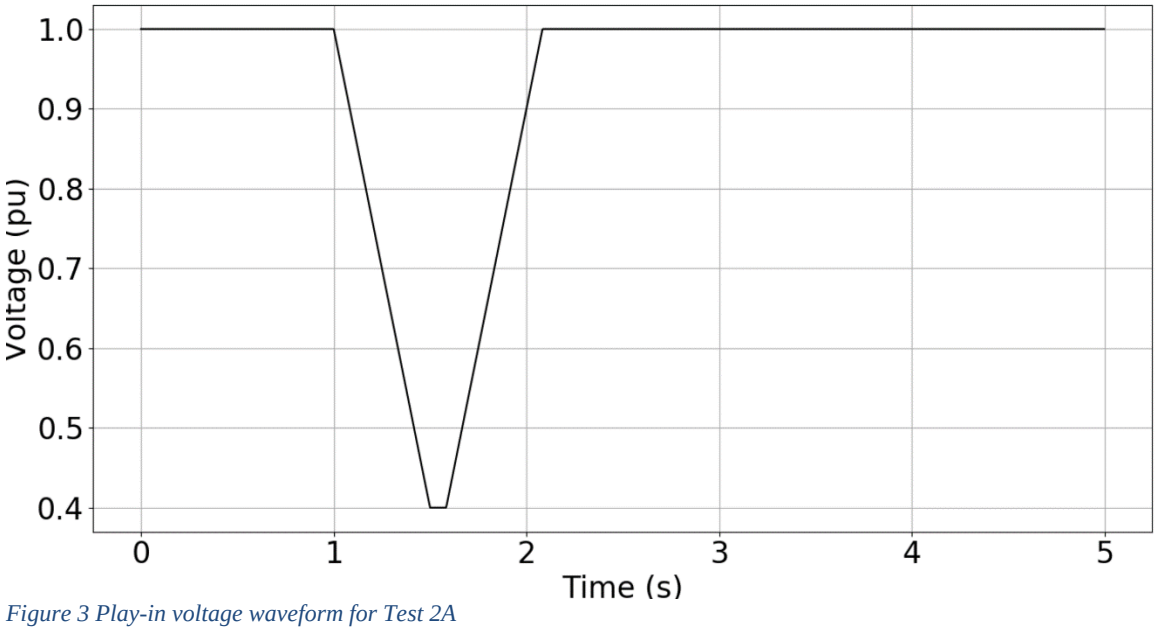

Figure 3 Play-in voltage waveform for Test 2A

Test Number 2B

The play-in waveform for this test is as shown in Figure 4. A voltage sag of 0.40 pu is applied at 1.0s for a duration of 5 cycles on 60 Hz. Immediately after that, the voltage is raised to 0.75 pu and ramped back to 1pu in 4s and run the simulation thereafter till 8s

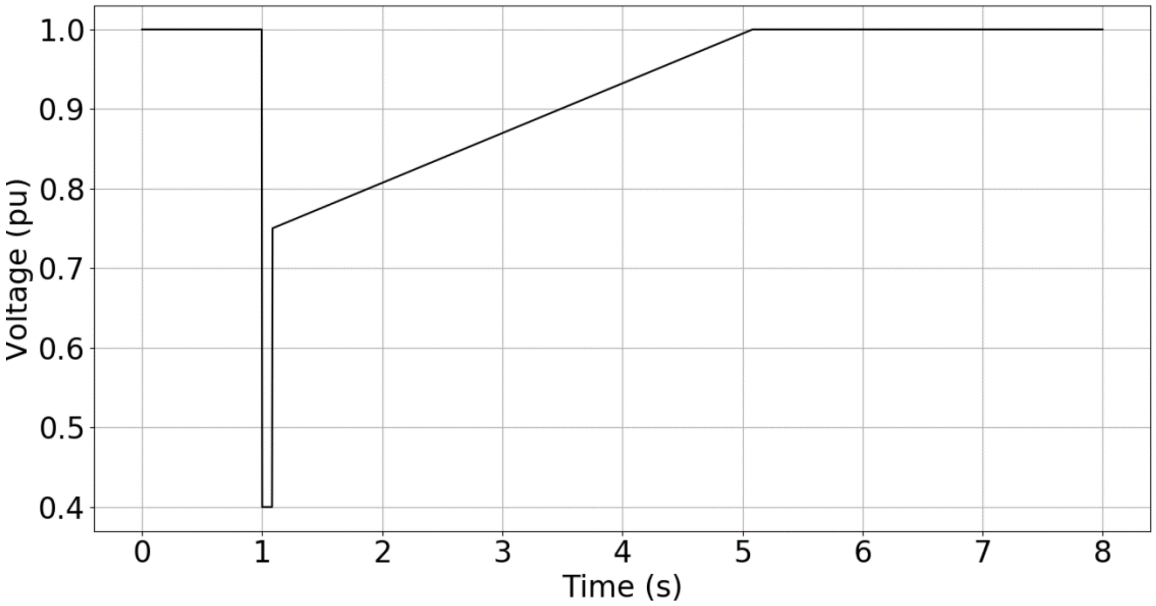

Figure 4 Play-in voltage waveform for Test 2B

Test Number 3

Figure 5 shows the frequency play-in waveforms to be used for test 3 while the equation provides details regarding the construction of the waveform

$$f(t) = \begin{cases} 60.0, & \text{for } 0.0 \le t < 1.0 \\ A + B\exp^{-C(t-1.0)}\cos(D(t-1.0)) + E\exp^{-C(t-1.0)}\sin(D(t-1.0)), & \text{for } t \ge 1.0 \end{cases}$$

The values of the parameters A – E in the equation are tabulated in Table 3.

Table 3 Details of test frequency waveform

Test	A	B	C	D	E
3	59.94	0.06	0.199	0.3178	-1.8246

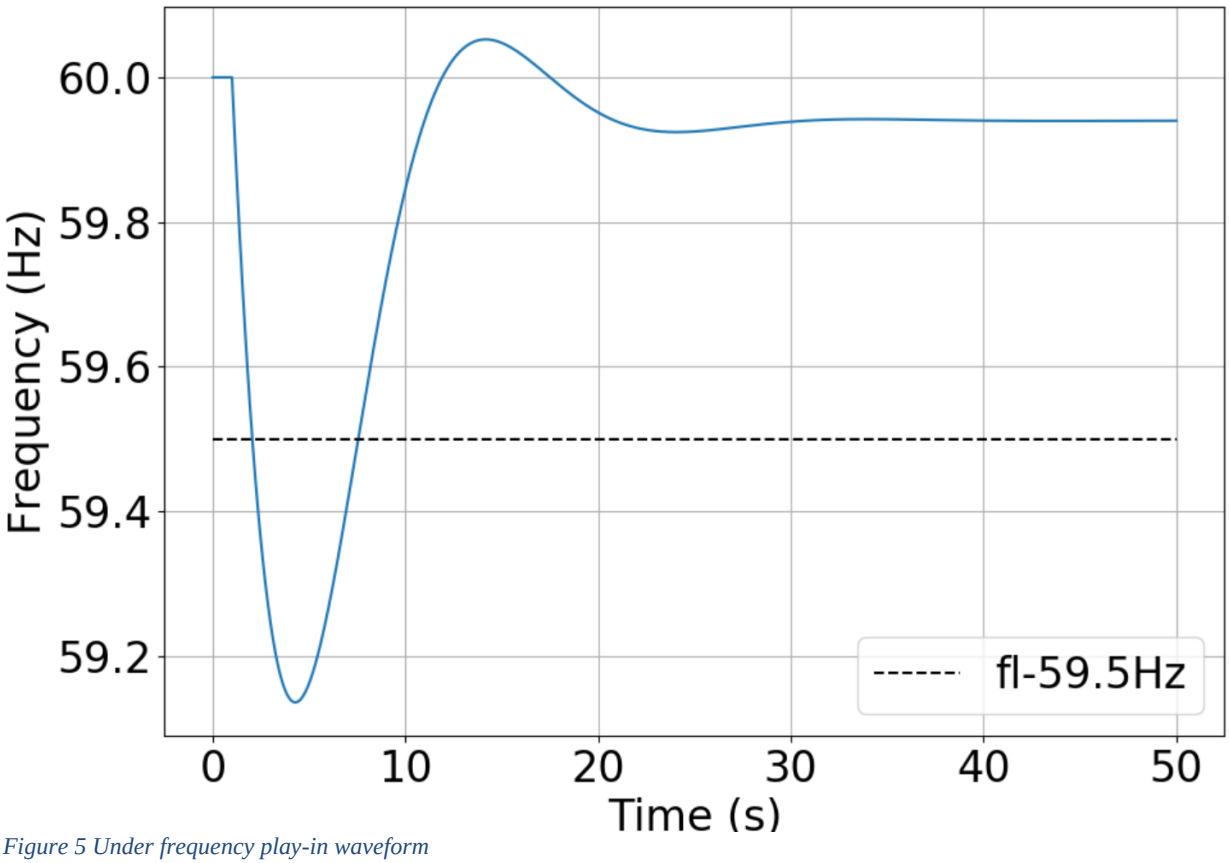

Figure 5 Under frequency play-in waveform

Test Number 4

The source at Bus 1 is represented by a classical machine model with MVA = 10000.0, H = 5.0s, and X" = 0.2pu.

References

[1] Bill Price and Shruti Rao, "CMPLDWG - DER-A Addition," WECC MVWG Meeting and NERC LMTF Meeting, January 2018 (https://www.nerc.com/comm/PC/LoadModelingTaskForceDL/CMPLDW_DER_A_Addition.pdf)

The parameter values for the DER_A model are provided in **Error! Reference source not found.**. For the rest of the composite load model, NERC default parameters with stalling enabled will be used

Table 4 Parameter values for DER_A model

DESCRIPTION	UNITS	Value	DESCRIPTION	Value
Trv	(s),	0.02	PfFlag; 1: constant power factor, 0: constant Q control	1
dbd1	(pu),	-0.05	FreqFlag; 1: frequency control enabled, 0: frequency control disabled	1
dbd2	(pu),	0.05	PQflag; 1: P priority for current limit, 0: Q-priority	0
Kqv	(pu/pu),	5	typeflag; 0: unit is a generator, 1: unit is a storage device	0
Vref0	(pu),	0.0	Vtripflag (flag to enable/disable voltage trip logic); 1: enable, 0: disable	1
Tp	(s),	0.02	Ftripflag (flag to enable/disable frequency trip logic); 1: enable, 0: disable	1
Tiq	(s),	0.02		
Ddn	(pu),	20.0		
Dup	(pu),	20.0		
fdbd1	(pu),	-0.000283		
fdbd2	(pu),	0.000283		
femax	(pu),	99		
femin	(pu),	-99	All (pu) values for this model are on a 12.47kV and 15.0 MVA base	
PMAX	(pu),	1.1		
PMIN	(pu),	0		
dPmax	(pu/s),	0.5		
dPmin	(pu/s),	-0.5		
Tpord	(s),	0.02		
Kpg	(pu),	0.1		
Kig	(pu),	10		
Imax	(pu),	1.2		
vl0	(pu),	0.5		
vl1	(pu),	0.88		

vh0	(pu),	1.2
vh1	(pu),	1.1
tvl0	(s),	0.1
tvl1	(s),	0.2
tvh0	(s),	0.1
tvh1	(s),	0.2
Vrfrac,	fraction	0.7
fl	(Hz),	59.5
fh	(Hz),	60.07
tfl	(s),	0.5
tfh	(s),	7.1
Tg	(s),	0.02
rrpwr	(pu/s),	0.5
Tv	(s),	0.02
Xe	(pu),	0.2
Iqh1	(pu)	0.5
Iql1	(pu)	-0.5
Vpr	(pu)	0.8