Generic Static Var System Models for the Western Electricity Coordinating Council

*Prepared by the WECC Static Var Compensator Task Force,*

*of the Modeling and Validation Working Group*

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ACKNOWLEDGEMENTS

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We also gratefully acknowledge other vendors and interested parties that have corresponded with this group (i.e., copied on the e-mail list and thus at least followed the work and provided feedback from time to time). These include American Superconductor (AMSC), Areva Transmission & Distribution and S&C Electric Company.

Sincere gratitude is due to the software vendors who have adopted models that were developed and implemented them in their standard model libraries, namely GE and Siemens PTI. Of course, in the process GE and Siemens PTI thus significantly contributed to the whole effort. We look forward to other software vendors adopting these models.

Finally, we gratefully acknowledge WECC and the WECC Modeling and Validation Working Group for inspiring and promoting this work. NERC’s presence and input in our Task Force meetings is also gratefully acknowledged.

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- Philippe Maibach, ABB
- John Paserba, Mitsubishi
- William Price, Consultant
- Mark Reynolds, Siemens
Bangalore Vijayraghavan, PG&E
Reza Yousefi, PG&E
1 INTRODUCTION

This is a report of the work of the WECC Static Var Compensator (SVC) Task Force (TF) of the WECC Modeling and Validation Working Group.

The mission statement of the SVCTF is:

Invest best efforts to accomplish the following:

- Improve power flow and dynamic representation of Static Var Systems (SVS) in positive-sequence simulation programs with a focus on generic, non-proprietary power flow and dynamic models. An SVS is defined as a combination of discretely and continuously switched Var sources that are operated in a coordinated fashion by an automated control system. This includes SVCs and STATCOMs.

- The models should be suitable for typical transmission planning studies. Power flow models should be suitable for both contingency and post-transient analyses. Dynamic models should be valid for phenomena occurring in a timeframe ranging from a few cycles to many minutes, with dynamics in the range of 0.1 to 10 Hz, and simulated with a time step no smaller than ¼ cycle.

- To develop a modeling guideline document.

- To collaborate with manufacturers and other stakeholders, IEEE, CIGRE, EPRI, etc.

The goal of the SVCTF is to develop more comprehensive models to better represent both existing and future SVS installations. In all modeling efforts, there is always a balance to be achieved between detail and flexibility. The SVCTF is developing a generic, non-proprietary model that is flexible enough for use in modeling existing facilities and newly proposed SVS. It is fully realized that it would not be possible for such a model to cater to every conceivable configuration of equipment and control strategy. Occasionally, some additional user-written supplemental controls may be needed to augment the models presented here.

More specifically the SVCTF is developing:

1. A generic SVS model for a thyristor-controlled reactor (TCR)-based SVC to be coordinated with Mechanically Switched Shunt (MSS) devices.

2. A generic SVS model for a TSC/TSR-only based SVC coordinated with MSSs.

3. A generic SVS model for a voltage source converter (VSC) based STATCOM coordinated with MSSs.
4. Enhanced power flow models that at minimum will capture the:
   a. Coordinated MSS switching logic based on susceptance.
   b. Slow-susceptance control feature of SVCs.
   c. Slope (droop or current compensation).

5. A directly associated dynamic SVS model with a switchable/controllable shunt model in power flow (rather than having to connect the dynamic model to a generator model).

To achieve the above goals, the following approach was taken:

   **Step 1** – develop a prototype dynamic model of the generic SVS (item 1 above) in GE PSLF™, as a user-written model, and verify its performance.

   **Step 2** – run some simulation tests on the model.

   **Step 3** – release the code publicly to allow its implementation as a standard model library item in GE PSLF™, Siemens PTI PSS/E™, and any other software tools. In parallel, extend the model to cover items 2 and 3 above (i.e., TSC/TSR-based and STATCOM-based SVS).

   **Step 4** – in parallel to all of the above, implement changes to develop a power flow algorithm to be implemented in GE PSLF™, Siemens PTI PSS/E™, and any other software platform that wishes to adopt it.

   **Step 5** – document the work.

The model developed here is heavily based on the documents listed in Section 5: References as [1], [2], [3], and [9]. The project was started with the code provided by Tucson Electric Power and Pacific Gas and Electric during meetings of the WECC SVCTF (which is code developed by ABB Inc.). This code has been modified to incorporate a few extra features discussed and presented during the SVCTF meetings [4], [5], and [6] in order to make the model more generic. One additional pertinent reference is [7].

The finalized code for the TSC/TCR-based SVC has been tested and approved, and released and thus implemented in the GE and Siemens PTI programs, and may be adopted by other vendors too.

The code associated with the document [9] has been generously provided to the SVCTF by ABB and thus passed along to GE and Siemens PTI (and other SVCTF members) to start the process of implementing it as the generic STATCOM dynamic model. The model was approved at the last SVCTF meeting.

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1 Positive Sequence Load Flow/GE PSLF Software
2 Siemens/Power Technologies International: Power System Simulator for Engineering
The document [10] was sent to the SVCTF by Siemens PTI as the first proposal for the TSC/TSR SVS dynamic model.

This document is a detailed account of the first and completed model, the TCR-based SVS, which is referred to as the svsmo1 model.
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2
THE GENERIC SVS MODEL

2.1 The Time-Domain Dynamic Models

Some Basic Assumptions
The intended use of the models presented here are for power system simulation studies in positive sequence stability programs. Furthermore, we are concerned with phenomena that:

- range typically between a few tens of milliseconds to tens of seconds
- have frequencies of 0.1 Hz to 3 Hz (inter-area to local modes of electromechanical oscillation)
- affect (occasionally) controller dynamics (i.e., stability of the voltage control loop) that may be in the 10 Hz or so range

The TCR-based SVS (SVSMO1)
This section documents the dynamic (time domain) generic model for an SVS that is comprised of a thyristor-based SVC potentially coupled with coordinated mechanically switched shunts (MSSs). Furthermore, it is assumed that at least one TCR branch exists. For the purpose of positive sequence simulations, the SVC can be modeled as a smoothly and continuously controllable susceptance throughout its entire range.

In developing the SVC model, the SVCTF made the following broad but reasonable assumptions:

1. The pertinent key control loops that should be modeled are:
   a. The voltage regulator
   b. The coordinated switching logic for MSSs
   c. The slow-susceptance regulator, if any
   d. Deadband control, if any
   e. SVC slope/droop
   f. SVC limits, over- and under-voltage strategy and voltage trip set points
   g. Any short-term rating capability

3 That is, allowing for either switched shunt capacitors or inductors.
2. What is not pertinent for modeling are:

   a. TCR and TSC current limits – for large transmission SVCs, the equipment will typically be specified to be able to deliver full reactive capability throughout the range of steady-state continuous primary voltage (system voltage), typically 0.9 pu to 1.10 pu. It is not expected that these current limiting devices will come into play for power system studies.

   b. Secondary Voltage Limitation – the secondary voltage on the low voltage side of the SVC step-up transformer may be limited by constraining the capacitive output of the SVC. Once again, the equipment will be typically specified to be able to deliver full reactive capability throughout the range of steady-state continuous primary voltage (system voltage), typically 0.9 pu to 1.10 pu. It is not expected that this limiting control will come into play for power system studies. This is not necessarily true for a STATCOM due to the more tightly controlled current limits and should typically be modeled for STATCOMs where necessary.

   c. Gain scheduler – this is typically some form of adaptive controller that adapts the open loop gain of the SVC to the particular system conditions. For example, if the system conditions become weak and result in the initiation of oscillations in the SVC voltage control loop (due to high open loop gain for the given condition), the gain scheduler will sense this and reduce the voltage regulator gain until the oscillations are suppressed.

   This constitutes too much detail for typical power system studies. The user should choose an appropriate gain to ensure stable closed-loop operation for the given network conditions being studied. Most studies look at N-1, N-1-1 and N-2 conditions. Such conditions do not typically lead to the extreme changes in network short circuit level that would initiate operation of the gain scheduler.

   d. Other main controls and details (cooling system controls, etc.) that have little to no bearing on system dynamic performance studies.
The final generic dynamic SVS model is shown below.

Figure 2-1: Generic model of an SVC-based SVS, assuming an SVC with at least one TCR branch.

The prominent features of the model are:

- **Proportional-Integral Primary Voltage Regulation Loop:** This is the heart of the SVC. Kpv and Kiv are the proportional and integral gain of the control loop. (Note: to be even more generic one could add an optional additional derivative gain; however, including derivative control is quite rare for large transmission SVCs). A word of caution for the user. The proportional gain of the proportional and integral (PI) regulator typically has a negative impact on any oscillations throughout the frequency range, which will have a negative effect on higher frequency oscillations whereas the gain of an integrating regulator will rapidly reduce with increasing frequency. The reason that a PID regulator is almost never used in flexible AC transmission systems (FACTS) devices is the rapid gain increase with frequency. This model only provides the ability to implement PI and I regulators. Even in this case the user should be cautious since positive sequence programs are not able to model network phenomena higher than about two or three Hz. What may appear as an attractive PI control in stability analysis

---

4 Proportional-integral-derivative regulator.
5 Integral regulator.
using a positive sequence simulation program, may have adverse effects on oscillation modes outside the simulation programs frequency range in practice. This requires knowledge from the user to be able to have the necessary judgment to provide proper tuning. Also, in special cases more detailed three-phase equipment level modeling and analysis may be needed, and should be coordinated with the equipment vendor. Note: in this model we assume that the integral gain is always non-zero.

**WARNING** – the user must be aware that if PI control is used in this stability-type model, excessive proportional gain may lead to undesired reduction in damping of network phenomena in higher frequency bands that are not modeled in stability programs (i.e., above the two–to-three Hz range).

- Power Oscillation Damper (POD), and the Voltage-based MSS Devices: These have separate control loops so they are separate supplemental models (see Figure 2-4 and 2-5).
- **Lead/Lag Block for Voltage Measurement:** The block with time constants $T_{c1}/T_{b1}$ represents the voltage measurement process.
- **Lead/Lag Block for Transient Gain Reduction:** The block with time constants $T_{c2}/T_{b2}$ can be used to introduce transient gain reduction or simply to experiment with the impact of SVC response on damping through phase lead compensation. Typically, it is not used.
- **Slow Susceptance Regulator:** The PI regulator $K_{ps}/K_{is}$ is the slow susceptance regulator that slowly biases the SVC reference voltage between the values of $v_{ref\text{max}}$ and $v_{ref\text{min}}$ to maintain the steady-state output of the SVC within the bandwidth of $B_{scs}$ and $B_{sis}$. The $B_{ref}$ control logic (see Figure 2-1) is as follows:

  - If $(B < B_{sis})$ then $B_{ref} = B_{sis} + \epsilon$
  - If $(B > B_{scs})$ then $B_{ref} = B_{scs} - \epsilon$
  - Otherwise $B_{ref} = B$

  Where $\epsilon$ is a small delta (e.g., 0.5 MVAR) to ensure that the slow susceptance regulator does not interact with the MSS switching, since typically first (larger delay) switching point of the MSSs is set to the same band as the slow susceptance regulator. Note: in the dynamics model the output of this regulator, $pio2$, is always initialized to zero.

- **Protection:** To protect the SVC equipment from prolonged overvoltage conditions, at excessive system voltages the SVC will trip after a given definite time delay. This is modeled. Also, since the TCR cooling system shuts down for prolonged under-voltage scenarios, the SVC will also trip after a prolonged low-voltage condition. This too is modeled. This is modeled by the parameters $UVT$, $UVtm2$, $OV2$, and $OVtm2$.
Over/Under-Voltage Strategy: In order to prevent overvoltage following the clearing of a close in fault, the under-voltage strategy is implemented. If the SVC bus voltage is less than a given value (for example, 0.6 pu – this is a tunable parameter and the setting is based on the studies and the need of the particular system, e.g., see [1]) the SVC susceptance is limited to the value of the fixed filter banks. If the voltage returns in less than a set time delay, then the SVC will continue normal operation; otherwise there is typically a 150 ms delay – this delay is to allow for the PLL to re-synchronize.

If the voltage falls below a more severe voltage level (e.g., 0.3 pu) then the SVC is forced to its inductive limit to prevent an overvoltage when the system voltage is restored. This is the under-voltage strategy and is modeled with the parameters UV1, UV2, UVtm1, and PLLDelay. During overvoltage conditions where the SVC bus voltage exceeds a given level, the SVC output is forced to its inductive limit. This is the overvoltage strategy and is modeled by the parameters OV1 and OVtm1.

Short-Term Rating: Short-term rating is modeled (that is, the SVC output can exceed its continuous rating up to a given amount for a short time period). This is modeled by the parameters Bshrt and Tshrt.

Optional Deadband Control: This is an optional deadband controller. The deadband control, slow susceptance regulator and non-linear droop are all intended for the same purpose – maintaining the SVC at a low steady-state output when the system voltage is within a given bandwidth. However, these three control strategies achieve this in quite different ways.

For stable and suitable control response, the use of any combination of deadband control, slow-susceptance regulation, and non-linear slope/droop is highly discouraged. Only one of the three should be used in the control strategy. The model checks for this conditions during initialization and does not allow the use of combinations of these controls.

The implementation of the deadband controller, as presented in the model, is not necessarily meant to represent the exact control strategy, but rather to be a generic representation of deadband control. The approach presented here ensures that the model initializes properly and within the deadband limits when one goes from powerflow to dynamics. The reference voltage of the SVC is taken to be the scheduled voltage at the bus from powerflow. Vdbd1 defines the deadband around this voltage.

If upon model initialization the bus voltage is found to be outside this range (i.e., outside Vschedule + Vdbd1 to Vschedule – Vdbd1) then the user is warned and Vref is set to the actual solved bus voltage – in order to prevent initialization problems with the model.

Non-Linear Slope/Droop: If the parameter flag2 is set to 0 then a standard linear droop of Xc1 is assumed, as is typical in most designs. Alternatively, by setting flag2 to 1, one can use a three piece piecewise linear droop setting. This can be
used to make the SVC non-responsive in a given bandwidth, similar to deadband control.

The logic for this is as follows (see Figure 2-1 and Figure 2-7):

```python
if ( flag2 = 0 )
    Xc = Xc1
else
    if ( Vr >= Vup )
        Xc = Xc1
    elseif ( (Vr < Vup) and (Vr > Vlow) )
        Xc = Xc2
    else
        Xc = Xc3
end
end
y = Xc*Isvc = Xc*V*B
```

This control is more susceptible to limit cycling if not properly tuned. Note: upon initialization, the model checks to make sure the initial SVC output is zero (0) MVar and that the initial bus voltage is in the middle of the range (i.e., \((V_{up} + V_{low})/2\), see Figure 2-5). This is a necessary condition for proper initialization.

- **MSS Logic:** Detailed MSS logic is implemented that allows for automated MSS switching based on SVC VAr output. Two thresholds (typically, one for fast switching and one for slow switching) are implemented with different delays on switching. The MSS discharge time can also be set (i.e., time the MSS must be switched out before it can be switched back in; this applies only to shunt capacitors). The MSS breaker delay is also modeled. Note: if used, MSS switching must be properly coordinated with the slow-susceptance regulator. Typically, to avoid excessive MSS switching, the slow-susceptance regulator time constant is chosen such that it acts first to bring the SVC to within the first threshold. If it is unable to achieve this, then the MSSs switch. The delay time on the first (smaller and slower) threshold for MSS switching is chosen to be significantly longer than the slow-susceptance time constant. Also, the slow-susceptance time constant is much longer than the primary voltage regulator loop response time.

- **The Lag Block (T2):** This represents the delay in the firing circuit of the SVC. Although in the past this has been modeled as a pure delay \(e^{-st}\) or a combination of a pure delay and lag block [7], here for the sake of simplicity the SVCTF has chosen to use a simple and single lag block. It should be noted that the susceptance feedback to the slope calculation is taken as the actual susceptance after the firing delay. In reality this susceptance may actually be the susceptance command or a measured value. Such nuances are not particularly important for the purposes of the modeling work here that is focused on power system stability analysis.
A supplemental damping controller can be connected to the main model at $V_{sig}$ (see Figure 2-1) shows the block diagram of a generic damping controller that can be provided as a separate supplemental control model to be hooked into the main SVS model.

Figure 2-4 illustrates a case that was simulated with and without the generic POD applied at the $V_{sig}$ input shown in Figure 2-1. The plot shows power oscillations on the remaining tie-line from bus 2 to 3 (in Figure A-1) when the second line is faulted and tripped. The generator models were tweaked to provide increased oscillations. The intent here is not to show how to tune a POD but simply that it works and can be applied to an SVC – more specifically the SVC model developed here. For more details on SVC POD tuning see references 17, 18 and 19 in Section 6.

Figure 2-2: Generic Damping Controller

![Generic Damping Controller Diagram](image)

Figure 2-3: Voltage-Based MSS switching (reproduced from [11] IEEE© 2006)

A separate stand alone switchable shunt model for shunt switching based purely on voltage set points (see Figure 2-3) is provided in GE PSLF™ and Siemens PTI PSS™E. This model simply allows for switching the shunt in (or out) once the voltage falls (or
rises) above a certain value for a given amount of time. It also models the discharge time required for a shunt capacitor (which can be set to either zero for reactors or to a small value for fast-discharge capacitors).

Figure 2-4: Illustration of the functioning of the POD.
Is $(V_{ref} - V_{dbd1}) < V_r < (V_{ref} + V_{dbd1})$?

- No
  - Release SVC

- Yes
  - Is $(V_{ref} - V_{dbd2}) < V_r < (V_{ref} + V_{dbd2})$ for more than $T_{dbd}$ seconds?
    - No
    - Yes (Lock SVC at present VAr output)
    - No

**Figure 2-5: Deadband control logic.**

<table>
<thead>
<tr>
<th>Connect MSC</th>
<th>Connect MSC</th>
<th>Disconnect MSC</th>
<th>Disconnect MSC</th>
</tr>
</thead>
<tbody>
<tr>
<td>fast strategy</td>
<td>slow strategy</td>
<td>slow strategy</td>
<td>fast strategy</td>
</tr>
<tr>
<td>$t_{delay} = 200ms$</td>
<td>$t_{delay} = 120s$</td>
<td>$t_{delay} = 120s$</td>
<td>$t_{delay} = 200ms$</td>
</tr>
</tbody>
</table>

$B_{svc}$ [p.u.]

-2.4 -1.6 capacitive
-0.8 0 0.4 inductive
0.8 1.0

**Figure 2-6: Example of the settings for the MSS switching logic based on SVC susceptance (from [8], © IEEE 2006).**
Figure 2-7: Non-linear droop
**SVSMO1 Model Parameters:**

The table provided below shows all the parameters of `svsmo1`. Each parameter is explained and a typical range of values provided. Where “N/A” is listed in the typical range of values column, this means that the value is based on specifications, design and tuning and so a typical range is really not applicable to this parameter. The model is per unitized on the SYSTEM MVA BASE. In North America, typically a system MVA base of 100 MVA is used. So for example, the Bmax for a 240 MVAR/-100 MVAR SVC would be 2.4 pu on 100-MVA base.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Typical Range of Values</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>vrefmax$^6$</td>
<td>The maximum allowable voltage reference setpoint of the AVR</td>
<td>1.04 to 1.06 pu</td>
<td>pu</td>
</tr>
<tr>
<td>vrefmin</td>
<td>The minimum allowable voltage reference setpoint of the AVR</td>
<td>0.99 to 1.01 pu</td>
<td>pu</td>
</tr>
<tr>
<td>UVSBmax</td>
<td>Maximum capacitive limit of the SVC during undervoltage strategy</td>
<td>Typically the total shunt capacitance of the fixed filter banks</td>
<td>pu</td>
</tr>
<tr>
<td>UV1</td>
<td>Under voltage setpoint 1</td>
<td>N/A</td>
<td>pu</td>
</tr>
<tr>
<td>UV2</td>
<td>Under voltage setpoint 2</td>
<td>N/A</td>
<td>pu</td>
</tr>
<tr>
<td>UVT</td>
<td>Under voltage trip setpoint</td>
<td>N/A</td>
<td>pu</td>
</tr>
<tr>
<td>OV1</td>
<td>Over voltage setpoint 1</td>
<td>N/A</td>
<td>pu</td>
</tr>
<tr>
<td>OV2</td>
<td>Over voltage setpoint 2</td>
<td>N/A</td>
<td>pu</td>
</tr>
<tr>
<td>UVTm1</td>
<td>Under voltage time 1 (see PLL delay for explanation)</td>
<td>N/A</td>
<td>s</td>
</tr>
<tr>
<td>UVTm2</td>
<td>Under voltage trip time (time after which SVC trips when V &lt; UVT)</td>
<td>N/A</td>
<td>s</td>
</tr>
<tr>
<td>OVtm1</td>
<td>Over voltage trip time 1</td>
<td>N/A</td>
<td>s</td>
</tr>
<tr>
<td>OVtm2</td>
<td>Over voltage trip time 2</td>
<td>N/A</td>
<td>s</td>
</tr>
<tr>
<td>mssbus</td>
<td>Bus number in the powerflow where the MSSs are located</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Mssid1</td>
<td>Id of the first MSS</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Mssid2</td>
<td>Id of the second MSS</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Mssid3</td>
<td>Id of the third MSS</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Mssid4</td>
<td>Id of the fourth MSS</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Mssid5</td>
<td>Id of the fifth MSS</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Mssid6</td>
<td>Id of the sixth MSS</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Mssid7</td>
<td>Id of the seventh MSS</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Mssid8</td>
<td>Id of the eighth MSS</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>flag1</td>
<td>0 – no switching of MSS; 1 – MSS switching enabled</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>flag2</td>
<td>0 – linear slope; 1 – non-linear slope</td>
<td>0</td>
<td>N/A</td>
</tr>
</tbody>
</table>

---

$^6$ vrefmax/vrefmin in GE PSLTTM are modeled in the powerflow data card.
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xc1</td>
<td>Slope (nominal linear slope; first part of piecewise linear slope)</td>
<td>0.01 to 0.05 pu/pu</td>
</tr>
<tr>
<td>Xc2</td>
<td>Slope of second section of piecewise linear slope</td>
<td>N/A pu/pu</td>
</tr>
<tr>
<td>Xc3</td>
<td>Slope of third section of piecewise linear slope</td>
<td>N/A pu/pu</td>
</tr>
<tr>
<td>Vup</td>
<td>Upper voltage break-point of non-linear slope</td>
<td>N/A pu</td>
</tr>
<tr>
<td>Vlow</td>
<td>Lower voltage break point of non-linear slope</td>
<td>N/A pu</td>
</tr>
<tr>
<td>Tc1</td>
<td>Voltage measurement lead time constant</td>
<td>0 s</td>
</tr>
<tr>
<td>Tb1</td>
<td>Voltage measurement lag time constant</td>
<td>0.025 – 0.05 s</td>
</tr>
<tr>
<td>Tc2</td>
<td>Lead time constant for transient gain reduction</td>
<td>0 s</td>
</tr>
<tr>
<td>Tb2</td>
<td>Lag time constant for transient gain reduction</td>
<td>0 s</td>
</tr>
<tr>
<td>Kpv</td>
<td>Voltage regulator proportional gain</td>
<td>0 pu/pu/s</td>
</tr>
<tr>
<td>Kiv</td>
<td>Voltage regulator integral gain</td>
<td>50 – 500 pu/pu</td>
</tr>
<tr>
<td>Vemax</td>
<td>Maximum allowable voltage error</td>
<td>N/A (typically set to 999 to ignore) pu</td>
</tr>
<tr>
<td>Vemin</td>
<td>Minimum allowable voltage error</td>
<td>N/A (typically set to -999 to ignore) pu</td>
</tr>
<tr>
<td>T2</td>
<td>Firing delay time constant</td>
<td>0.005 – 0.01 s</td>
</tr>
<tr>
<td>Bshrt</td>
<td>Short-term maximum capacitive rating of the SVC</td>
<td>N/A pu</td>
</tr>
<tr>
<td>Bmax</td>
<td>Maximum continuous capacitive rating of the SVC</td>
<td>N/A pu</td>
</tr>
<tr>
<td>Bmin</td>
<td>Minimum continuous inductive rating of the SVC</td>
<td>N/A pu</td>
</tr>
<tr>
<td>Tshrt</td>
<td>Short-term rating definite time delay</td>
<td>N/A s</td>
</tr>
<tr>
<td>Kps</td>
<td>Proportional gain of slow-susceptance regulator</td>
<td>0 pu/pu</td>
</tr>
<tr>
<td>Kis</td>
<td>Integral gain of slow-susceptance regulator</td>
<td>0.0005 – 0.001 pu/pu/s</td>
</tr>
<tr>
<td>Vrmax</td>
<td>Maximum allowed PI controller output of slow-susceptance regulator</td>
<td>0.05 – 0.1 pu</td>
</tr>
<tr>
<td>Vrmin</td>
<td>Minimum allowed PI controller output of slow-susceptance regulator</td>
<td>-0.1 – -0.05 pu</td>
</tr>
<tr>
<td>Vdbd1</td>
<td>Steady-state voltage deadband; SVC is inactive between Vref+Vdbd1 to Vref-Vdbd1</td>
<td>N/A pu</td>
</tr>
<tr>
<td>Vdbd2</td>
<td>Inner deadband; i.e., when SVC goes outside of Vdbd1, it must come back within the range Vref+Vdbd2 to Vref-Vdbd2 for Tdbd seconds in order for the SVC to be locked again in side Vdbd1.</td>
<td>One fifth to one tenth Vdbd1 pu</td>
</tr>
<tr>
<td>Tdbd</td>
<td>Definite time deadband delay</td>
<td>0.1 – 0.5 seconds s</td>
</tr>
<tr>
<td>PLLdelay</td>
<td>PLL delay in recovering if voltage remains below UV1 for more than UVTm1</td>
<td>0.1 s</td>
</tr>
<tr>
<td>Eps</td>
<td>Small delta added to the susceptance bandwidth of the slow-susceptance regulator in order to ensure its limits are not exactly identical to the MSS switching point</td>
<td>0.1 MVAr</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Value 1</td>
</tr>
<tr>
<td>---------</td>
<td>------------------------------------------------------------------------------</td>
<td>---------</td>
</tr>
<tr>
<td>Blcs</td>
<td>Large threshold for switching MSS on the capacitive side</td>
<td>N/A</td>
</tr>
<tr>
<td>Bscs</td>
<td>Small threshold for switching MSS on the capacitive side</td>
<td>N/A</td>
</tr>
<tr>
<td>Blis</td>
<td>Large threshold for switching MSS on the inductive side</td>
<td>N/A</td>
</tr>
<tr>
<td>Bsis</td>
<td>Small threshold for switching MSS on the inductive side</td>
<td>N/A</td>
</tr>
<tr>
<td>Tmssbrk</td>
<td>MSS breaker switching delay (for opening and closing; assume the same for all MSS)</td>
<td>N/A</td>
</tr>
<tr>
<td>Tdelay1</td>
<td>Definite time delay for larger threshold switching</td>
<td>0.2 – 0.5</td>
</tr>
<tr>
<td>Tdelay2</td>
<td>Definite time delay for small threshold switching</td>
<td>120 – 300</td>
</tr>
<tr>
<td>Tout</td>
<td>Discharge time for mechanically switched capacitors</td>
<td>300</td>
</tr>
</tbody>
</table>

7 The MVAr values here for the MSS switching points really refer to a susceptance. That is, if we set Blcs = 100 MVAr, what we really mean is when the SVC susceptance goes above 1 pu on a 100-MVA base (i.e., the susceptance at which for 1 pu voltage the SVC output would be 100 MVAr) an MSS will be switched.
2.2 The Powerflow Model

The Powerflow Model for the Thyristor-based SVS

The following is the specification of the powerflow model for emulating a TCR-based SVS:

1. Allow connection of a shunt static var device model in powerflow directly to a dynamic model – this is an internal programming change.

2. Represent slope (ONLY LINEAR SLOPE).

Add one more parameter to the shunt data card – the linear slope (Xs) (ratio of voltage change to current change over the defined control range of the SVC).

If a three percent voltage change is allowed across the entire control range of the SVC operation and the SVC is rated +200/-100 MVAR and assuming system MVA base of 100 MVA, then the slope is 0.03/3 = 0.01 pu.

Note: IEEE Guide 1031 has pu based upon the entire range and this is widely used by the manufacturers, but because the models commonly handle MVA in pu on a 100-MVA base, the models use the 100-MVA base.

Actual bus voltage schedule (internal to the power flow solution) becomes:

\[ V_{\text{ref}} = V_{\text{sched}} + X_s \times B_{\text{svc}} \times V_{\text{bus}} = V_{\text{sched}} + I_{\text{svc}} \]

3. Represent the coordinated MSS switching (based on B). Allow eight MSS devices on up to eight buses.

- Add a parameter to allow the ability of the SVC for switching the MSSs to be turned on or off. Also, the SVC model will require two parameters that define the switching points for the MSSs; i.e., Bminsh and Bmaxsh, such that if the SVC B is greater than Bmaxsh a shunt capacitor (reactor) is switching in (out), and if it is less than Bminsh a shunt reactor (capacitor) is switched in (out).

- Model the MSS each separately in the shunt table. For each one add the following parameters:
  - A parameter that points to the controlling SVC
  - A parameter that indicates whether this MSS is available (1) or not (0) for remote switching by the SVC
  - A parameter that defines the ID of the controlling SVC

In actual practice, typically the shunt switching sequence is rotated to evenly distribute the switching operations among the shunts. For simulation work this is not important. For the purposes of simulation work, this document will switch the
shunts in the order they appear in the parameter list (skipping over those already in/out of service when trying to switch in/out a new shunt).

4. If a shunt control is strictly voltage-based and separate from the SVC, keep it in a separate model (both in powerflow and dynamics).

5. Represent the slow susceptance regulator to model this the following parameters are needed:

   o One parameter to turn this function on or off.
   o Two parameters (Bminsb and Bmaxsb) to define the range of B within which the SVC output is to be kept in steady-state.
   o Two parameters (Vrefmax and Vrefmin) to define the range of allowable voltage reference change by the SVC to keep the B output within Bminsb/Bmaxsb (see explanation of slow-susceptance regulator in the previous section or [1]).
   o A parameter for the user to define the approximate $\frac{\partial V}{\partial Q}$ at the bus where the SVC is located. This can be estimated from the short-circuit impedance at the bus. The reason for this parameter is explained below in the algorithm explained here and taken from the code developed in [2].

The proposed algorithm is as follows:

vrefmax (maximum allowable voltage schedule at the bus)

vrefmin (minimum allowable voltage schedule at the bus)

First solve the powerflow for one iteration to hold the current bus scheduled voltage (including slope)

If (slow susceptance on)

    If $B_{maxsb} < B_{svc} < B_{minsb}$
        take no action
    else
        lower/raise vsched (bus scheduled voltage) until SVC output is between $B_{maxsb}/B_{minsb}$ as proposed below (1).
        vsched must ALWAYS be between vrefmax & vrefmin, i.e., if it hits one of these limits then stop.

end

end
(1) from the input by the user we have $V_{\text{grad}} = \left[\partial V/\partial Q\right]^{-1}$. Now change $v_{\text{sched}}$ as follows:

$$v_{\text{sched}} = v_{\text{sched}} + (B_{\text{maxsb}} - B_{\text{svc}}) \times (1/V_{\text{grad}})$$

iterate until it converges.

The following diagram depicts the steady-state behavior of the slow-susceptance regulator.

An important note for the user is to understand that the actual bus voltage, after convergence of the powerflow solution, may not be exactly equal to the scheduled voltage ($V_{\text{sched}}$). If a proper powerflow solution is reached, the reason for this difference is driven by two actions of the SVS controls: (i) a non-zero slope ($X_s$), and (ii) the action of the slow-susceptance regulator, which deliberately acts to bias the scheduled voltage to bring the steady-state output of the SVC to within the desired steady-state reactive power output bandwidth ($B_{\text{minsb}}$ and $B_{\text{maxsb}}$) – see Figure 2-1.
MODEL VALIDATION

Model Validation to Date

The model presented here is based on the one reported in [1], [2] and [8]. The main difference is in the addition of some of the more generic features:

1. deadband control
2. non-linear slope/droop
3. the extra lead/lag block

Apart from these features, the core of the model is essentially identical to those in [1], [2], and [8].

In [1], the model was validated against a detailed vendor PSCAD™ model of the actual SVC controls. In [8], the model was verified against an actual DFR recording of the SVC response following a major system disturbance. In this case, many of the salient features of the model were verified; the under-voltage strategy, the slope, the main voltage regulation loop, etc.

In summary, this model is quite suitable for use in power system simulation and can reliably capture all the relevant dynamics of a modern SVC system.

Figure 3-1: Example model validation (from [8], © IEEE 2006).
Further Model Testing/Validation

The data for the above event — the digital fault recorder (DFR) recording — was provided by ABB to EPRI. Using a similar technique to that described in [12], the DFR data was used by to validate the SVS model shown in Figure 2-1. By feeding the measured transmission system voltage into the model and fitting the susceptance and Q (reactive power) response – see Figure 2 – the model was validated. This illustrates an example of model validation for a FACTS device. The recorded response of the SVC was captured by the digital fault recorder (DFR) that is built-in the SVC control system.

Figure 3-2: Measured and simulated reactive power output response of a transmission SVC installation. Response is to a delayed clearing of a transmission fault (see [8] for a description of the event).

Similarly, ABB provided data for another system event for a different SVC installation. This too was easily validated, see Figure 3-3.
Figure 3-3: Measured and simulated reactive power output response of a transmission SVC installation. Response is to a WECC-wide event.
4
FURTHER WORK

The key work that remains for the WECC SVCTF is as follows:

1. To review, approve, and finalize the proposed TSC/TSR-based SVS model and then have it implemented in the programs.

2. To finalize the dynamic model for the VSC-based SVS.

3. To finalize the powerflow model for the VSC-based SVS.
5
REFERENCES


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FURTHER READING AND OTHER USEFUL REFERENCES


14. CIGRE Technical Brochure 77, *Analysis and optimization of SVC use in transmission systems*, CIGRE Task Force 38.05.04, 1993


SVC DYNAMIC MODEL TESTING FOR THE TCR-BASED SVS MODEL

1.0 Objective

The objective of this task is to test and validate the features and performance of a generic SVC dynamic model.

This test plan should be considered a supplement to the “Generic SVC Model for WECC” document prepared by the WECC SVC Modeling Task Force of the Modeling and Validation Working Group.

2.0 Description/Specification Benchmark test system

The test system is depicted in Figure A-1 below.

![Figure A-1. Simplified One-Line for Test System Model](image)

The following are characteristics of the test system model:

1) Bus 6 is the swing bus at 1.0 pu.

2) Generator 1 and 2 each has an exciter model and generator dynamic model.

   \[
   \text{exciter = exst4b, generator = genrou}
   \]

   \[
   G1 = G2 = P_{\text{max}}, \frac{Q_{\text{max}}}{Q_{\text{min}}} = 150 \text{ MW, } +/- 45 \text{ MVAr}
   \]

3) Each line segment is modeled as a 25-mile overhead transmission line.

   Line 11 Impedance = \(12 = 21 = 22\) => \(R, X, B = 0.003 \text{ pu, 0.0332 pu, 0.051 pu (Z_{\text{base}}=529\Omega)}\)
Line 31 Impedance = 32 = 41 = 42 => R,X,B = 0.023pu, 0.134 pu, 0.0152 pu (Zbase=132Ω)

4) The load composition at bus 2 and 4 is 40% induction motor and 60% static.

Load 1 = Pload, Qload = 100 MW, 30 Mvar
Load 2 = Pload, Qload = 115 MW, 30 Mvar

5) The transformer impedance(s) at bus 3 is 0.0564 pu on 252 MVA.

6) The SVC rating is -50/+200 Mvar connected at 230 kV (bus 7). The SVC is modeled as a generator in the powerflow with Qmin and Qmax set at SVC rating (-50/+200 Mvar). The scheduled voltage to achieve near zero output is 1.006 pu.

Figure 2-1 shows the general block diagram of the generic SVC model under test.

The following features of the generic SVC dynamic model are to be tested:

1) PI voltage regulation loop
2) Lead/lag voltage measurement (Tc1/Tb1)
3) Lead/lag for transient gain reduction (Tc2/Tb2)
4) Slow susceptance regulator
5) Over/undervoltage protection
6) Deadband control
7) Non-linear slope (droop)
8) MSS logic
9) Lag block (T2)
3.0 Case List

Table A-1 presents the overall case list for testing the generic SVC dynamic model being considered by the WECC SVC Modeling Task Force.

Table A-1 – Case List for Testing the Generic SVC Model

<table>
<thead>
<tr>
<th>Case Number</th>
<th>Event Description</th>
<th>Fault Location</th>
<th>Fault Impedance</th>
<th>Fault Clearing Time</th>
<th>Branch Cleared</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Fault</td>
<td>Bus 2</td>
<td>0</td>
<td>6 cycles</td>
<td>Line 22</td>
<td></td>
</tr>
<tr>
<td>1b</td>
<td>Fault</td>
<td>Bus 2</td>
<td>0.01+j0 pu</td>
<td>9 seconds</td>
<td>n/a</td>
<td>Test UV Trip</td>
</tr>
<tr>
<td>1c</td>
<td>Fault</td>
<td>Bus 2</td>
<td>0.1+j0.1 pu</td>
<td>9 seconds</td>
<td>n/a</td>
<td>Test UV Trip</td>
</tr>
<tr>
<td>2</td>
<td>Fault</td>
<td>Bus 3</td>
<td>0</td>
<td>6 cycles</td>
<td>TX2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Fault</td>
<td>Bus 5</td>
<td>0</td>
<td>6 cycles</td>
<td>Line 42</td>
<td></td>
</tr>
<tr>
<td>3a</td>
<td>Fault</td>
<td>Bus 5</td>
<td>0</td>
<td>6 cycles</td>
<td>Line 42</td>
<td>Illustrate slow voltage recovery</td>
</tr>
<tr>
<td>4</td>
<td>Fault</td>
<td>Bus 3</td>
<td>0</td>
<td>6 cycles</td>
<td>Line 21 &amp; Line 11</td>
<td>Unstable</td>
</tr>
<tr>
<td>5</td>
<td>Fault</td>
<td>Bus 4</td>
<td>0</td>
<td>6 cycles</td>
<td>Line 31 &amp; Line 41</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Step change</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td></td>
</tr>
<tr>
<td>6a-6e</td>
<td>Step change</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>Slope variation</td>
</tr>
<tr>
<td>7</td>
<td>Step change</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td></td>
</tr>
<tr>
<td>7a</td>
<td>Step change</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>Variation of Kpv/Kpi</td>
</tr>
<tr>
<td>8</td>
<td>Step change</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>Variation of Tc1/Tb1</td>
</tr>
<tr>
<td>8a</td>
<td>Step change</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>Variation of Tc1/Tb1</td>
</tr>
<tr>
<td>9</td>
<td>Step change</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>Variation of Tc2/Tb2</td>
</tr>
<tr>
<td>9a</td>
<td>Step change</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>Variation of Tc2/Tb2</td>
</tr>
<tr>
<td>10</td>
<td>Step change</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>Test Slow Susceptance Control</td>
</tr>
<tr>
<td>11</td>
<td>Inc Bus Voltage</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>Variation of overvoltage setting</td>
</tr>
<tr>
<td>12</td>
<td>Vary Bus Voltage</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>Test Deadband control</td>
</tr>
<tr>
<td>13</td>
<td>Vary Bus Voltage</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>Apply non-linear droop</td>
</tr>
<tr>
<td>14</td>
<td>Vary Bus Voltage</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>Switch MSSs</td>
</tr>
<tr>
<td>15</td>
<td>Step change</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>Variation of lag T2</td>
</tr>
<tr>
<td>16</td>
<td>Step change</td>
<td>Bus 2</td>
<td>0</td>
<td>6 cycles</td>
<td>Line 22</td>
<td>Apply POD control</td>
</tr>
</tbody>
</table>

NOTE: Refer to Table A-2 for a list of input model parameters and their settings for each case in Table A-1.
For all simulations, apply the following assumptions:

1) The fault is bolted and symmetrical (zero impedance, three-phase).
2) The fault occurs one second after the start of the simulation.
3) Run each simulation for at least 10 seconds.
4) At a minimum, simulation plots will include SVC susceptance and regulated bus voltage.
5) Model input parameters for each case are shown in Table A-2.

4.0 Test schedule

Initial testing: June 2008 (discussed at Edmonton, Alberta meeting)
Update report (r2): Sept 2008 (reviewed at Albuquerque, NM meeting)
Update report (r3): Nov 2008 (test new model code to switch shunt reactors)
Update report (r4): Jan 2009 (final report for review)
5.0 Simulation Results

Case 1 – Fault Bus 2 and Clear Line 22

Case 1 demonstrates the generic SVC model’s response to a fault near Bus 2 at 1 second in the simulation, with 6-cycle clearing of Line 22. Regulated bus voltage and SVC susceptance are shown in Figure A-2, with generator power swings shown in Figure A-3.

![Figure A-2. Case 1 simulation result; voltage, susceptance, and reactive power.](image)

![Figure A-3. Case 1 simulation result; power swings](image)
Case 1b – Fault Bus 2 and Test UV2 Trip

Case 1b demonstrates the generic SVC model’s response to a sustained fault near Bus 2 at 1 second in the simulation. The voltage fell below the UV2 threshold and then the UV2 timer elapsed after 7 seconds with voltage depressed. The SVC was then tripped off-line. Regulated bus voltage and SVC susceptance are shown in Figure A-4.

Figure A-4. Case 1b simulation result; undervoltage trip UV2
Case 1c – Fault Bus 2 and Test UV1 Trip

Case 1c demonstrates the generic SVC model's response to a sustained fault near Bus 2 at 1 second in the simulation. The voltage fell below the UV1 allowing the SVC output to be set to UVSBmax. The voltage continued down below UV2 and the SVC tripped off. Regulated bus voltage and SVC susceptance are shown in Figure A-5.

![Figure A-5. Case 1c simulation result; undervoltage trip UV1 and UV2](image-url)
Case 2 – Fault Bus 3 and Clear TX2

Case 2 demonstrates the generic SVC model’s response to a fault near Bus 3 at 1 second in the simulation, with 6-cycle clearing of Transformer 2. Regulated bus voltage and SVC susceptance are shown in Figure A-6, with generator power swings shown in Figure A-7.

![Figure A-6. Case 2 simulation result; voltage and susceptance.](image)

![Figure A-7. Case 2 simulation result; power swings](image)
Case 3 – Fault Bus 5 and Clear Line 42

Case 3 demonstrates the generic SVC model’s response to a fault near Bus 5 at 1 second in the simulation, with 6-cycle clearing of Line 42. Regulated bus voltage and SVC susceptance are shown in Figure A-8, with generator power swings shown in Figure A-9.

Figure A-8. Case 3 simulation result; voltage and susceptance.

Figure A-9. Case 3 simulation result; power swings.
Case 3a – Fault Bus 5 and Clear Line 42 with Delayed Voltage Recovery

Case 3a demonstrates the generic SVC model’s response to a fault near Bus 5 at 1 second in the simulation, with 6-cycle clearing of Line 42 generator excitation systems turned off and motor load increased from 40% to 99%. Regulated bus voltage and SVC susceptance are shown in Figure A-10.

![Case 3 simulation result; voltage and susceptance.](image)

**Figure A-10.** Case 3 simulation result; voltage and susceptance.
Case 4 – Fault Bus 3 and Clear Line 21 and Line 11

Case 4 demonstrates the generic SVC model’s response to a fault near Bus 3 at 1 second in the simulation, with 6-cycle clearing of Line 21 and Line 11. Regulated bus voltage and SVC susceptance are shown in Figure A-11.

Figure A-11. Case 4 simulation result.
Case 5 – Fault Bus 4 and Clear Line 31 and Line 41

Case 5 demonstrates the generic SVC model’s response to a fault at 1 second in the simulation near Bus 4 at 1 second in the simulation, with 6-cycle clearing of Line 31 and Line 41. Regulated bus voltage and SVC susceptance are shown in Figure A-12, with generator power swings shown in Figure A-13.

![Figure A-12. Case 5 simulation result; voltage and susceptance.](image1)

![Figure A-13. Case 5 simulation result; power swings.](image2)
**Case 6 – 2% Step Change**

Case 6 demonstrates the generic SVC model’s response to a 2% step change (increase) at 1 second in the simulation (slope=0.02).

The step change was implemented by adding the following EPCL code to the generic SVC model code:

```plaintext
@err = @vref - @vcomp

if (dypar[0].time >= 1.0) /* DJS CHANGE FOR STEP RESPONSE */
@err = @vref - @vcomp + 0.02 /* DJS CHANGE FOR STEP RESPONSE */
endif /* DJS CHANGE FOR STEP RESPONSE */
```

Regulated bus voltage and SVC susceptance are shown in Figure A-14.

(model filename: Generic_SVC_c2.p)

![Figure A-14. Case 6 simulation result; voltage and susceptance.](image)
Case 6 through 6e – Slope Variation

Case 6 through 6e illustrates the impact of varying the slope reactance (droop) from 0.01 to 0.1 for a 2% step change (increase) at 1 second in the simulation.

A comparison of regulated bus voltage for each slope variation is shown in Figure A-15.

(model filename: Generic_SVC_c2.p)

Figure A-15. Impact of slope variation on voltage response.
Case 7 – 2% Step Change and Vary Kpv/Kiv

Case 7 and Case 7a demonstrates the generic SVC model's response to a 2% step change (increase) at 1 second in the simulation with the proportional and integral gains of the voltage regulator increased.

- Kpv increased from 50 to 100 (Case 7)
- Kiv increased from 250 to 500 (Case 7a)

The result was then compared to Case 6, and is shown in Figure A-16 and Figure A-17.

**Figure A-16.** Case 7 simulation result compared to Case 6; voltage.

**Figure A-17.** Case 7 simulation result compared to Case 6; susceptance.
Figure A-17. Case 7 simulation result compared to Case 6; susceptance.
Case 8 – 2% Step Change and Vary Tc1/Tb1

Figure 8a and Figure 8b demonstrates the generic SVC model’s response to a 2% step change (increase) at 1 second in the simulation with the lead and lag voltage measurement time constant increased.

\[
\frac{1 + sTc1}{1 + sTb1}
\]

- Tb1 is 0.01, and Tc1 is zero (Case 6)
- Tb1 is 0.01, and Tc1 increased from 0 to 0.05 (Case 8)
- Tb1 increased from 0.01 to 0.08, and Tc1 is zero (Case 8a)

The result was then compared to Case 6, and is shown in Figure A-18 and Figure A-19.

Figure A-18. Case 8 simulation result compared to Case 6; voltage.
Figure A-19. Case 8 simulation result compared to Case 6; susceptance.
Case 9 – 2% Step Change and Vary Tc2/Tb2

Case 9 and Case 9a demonstrates the generic SVC model’s response to a 2% step change (increase) at 1 second in the simulation with the lead and lag transient gain time constants measurement time constant increased.

\[
\frac{1 + sTc_2}{1 + sTb_2}
\]

- Tb2 is zero, and Tc2 is zero (Case 6)
- Tb2 increased from 0 to 0.05, and Tc2 increased from 0 to 0.10 (Case 9)
- Tb2 increased from 0 to 0.05, and Tc2 is zero (Case 9a)

The result was then compared to Case 6, and is shown in Figure A-20 and Figure A-21.

**Figure A-20. Case 9 and 9a simulation results compared to Case 6; voltage.**
Figure A-21. Case 9 and 9a simulation results compared to Case 6; susceptance.
Case 10 – Step Change and With Slow Susceptance Control

Case 10 demonstrates the generic SVC model’s response to a 2% step change (increase) at 1 second in the simulation with the slow susceptance control activated. The slow susceptance control loop shown below should work to reduce the SVC’s output to within +/- 10 Mvar for this simulation case.

- $V_{rmin}$ and $V_{rmax}$ were changed from zero to +/- 0.5
- $B_{in2}$ and $B_{out2}$ were set to +10 Mvar and -10 Mvar

The result of Case 10 was then compared to Case 6, this is shown in Figure A-22.

Figure A-22. Case 10 simulation result
Case 11 – Test Overvoltage Trip

Case 11 demonstrates the generic SVC model’s response and subsequent trip resulting from a voltage increase (switching on 30 Mvar capacitor) simulated at 1 second in the simulation.

- OV1 was decreased from 1.3 to 1.03
- Bmin was decreased from -0.50 pu to -0.05

The SVC was tripped by OV1 threshold being exceeded for the time delay specified in parameter OVtm1, as shown in Figure A-23.

Figure A-23. Case 11 simulation result
Case 12 – Test Deadband Control

Case 12 demonstrates the generic SVC model's response to intentional variations in the regulated bus by MSS capacitor switching with the voltage deadband control activated.

This case was re-simulated with the voltage deadband turned off.

The voltage was varied with the following capacitor switching operation:

- 0 sec – no capacitors on
- 1-5 sec – two capacitors switched on (total 2x30 Mvar)
- 5-10 sec – one capacitor switched on (total 3x30 Mvar)
- 10-15 sec – two capacitors switched off (total 1x30 Mvar)
- 15-20 sec – one capacitor switched on (total 2x30 Mvar)

With the deadband control activated, the following control parameters were applied:

- CONT_Vdbd1 was set at 0.04
- CONT_Vdbd2 was set at 0.02
- CONT_Vdbd was set at 1 second

Figure A-24 illustrates the operation of the deadband control function, with Figure A-25 illustrating the same case without the deadband control activated. Figures A-26 and A-27 compare the two cases.

Figure A-24. Case 12 simulation result – with deadband control activated
Figure A-25. Case 12 simulation result – **without** deadband control activated

Figure A-26. Case 12 – **comparing** B svc with and without deadband control.
Figure A-27. Case 12 – comparing regulated bus voltage with and without deadband control
Case 13 – Test Non-Linear Slope

For Case 13, the simulation from Case 12 was rerun with the non-linear slope function activated.

With the non-linear control activated, the following control parameters were applied:

- flag1 set to 1
- CONT_Xc1 was set at 0.20
- CONT_Xc2 was set at 0.10
- CONT_Xc3 was set at 0.02
- CONT_Vup was set at 1.05
- CONT_Vlow was set at 0.95

Figure A-28 illustrates the operation of the non-linear slope control function, with Figures A-29 and A-30 illustrating the comparison between Case 13 and Case 12 (without deadband control).

Figure 5-28. Case 13 simulation result with non-linear slope activated.
Figure A-29. Voltage for Case 13 simulation compared to Case 12b (with no deadband control).

Figure A-30. Susceptance for Case 13 simulation compared to Case 12b (with no deadband control).
**Case 14 – Test MSS Switching**

Case 14 demonstrates the generic SVC model's capability to mechanically-switched shunt (MSS) devices such as capacitor banks based on reactive power output of the SVC. Intentional voltage variations were implemented to the regulated bus by changing Vsch through the dynamic simulation. There are four, 30 Mvar MSS devices available for switching in this simulation case.

The voltage was varied with the following capacitor switching operation:

- 0 sec – Vsch = 1.006 pu
- 1-20 sec – Vsch = 1.026 pu
- 20-40 sec – Vsch = 1.05 pu
- 40-60 sec – Vsch = 1.026 pu
- 60-80 sec – Vsch = 1.006 pu

With the MSS switching activated, the following control parameters were applied:

- flag1 = 1
- Bin1 was set at 40 Mvar (larger threshold for switching MSS)
- Bin2 was set at 20 Mvar (smaller threshold for switching MSS)
- Bout1 was set at -20 Mvar (larger threshold for switching MSS)
- Bout2 was set at -40 Mvar (smaller threshold for switching MSS)
- Tdelay1 was set to 0.5 seconds (delay for larger threshold)
- Tdelay2 was set to 3 seconds (delay for smaller threshold)

Figure A-31 illustrates the operation of the MSSs, including the scheduled voltage and the SVC’s susceptance.

- MSS 1 AT SVC SWITCHED IN AT TIME:4.821683
- MSS 2 AT SVC SWITCHED IN AT TIME:8.761267
- MSS 3 AT SVC SWITCHED IN AT TIME:22.289391
- MSS 4 AT SVC SWITCHED IN AT TIME:24.385181
- MSS 1 AT SVC SWITCHED OUT AT TIME:44.671082
- MSS 2 AT SVC SWITCHED OUT AT TIME:62.373989
- MSS 3 AT SVC SWITCHED OUT AT TIME:65.495934
Figure 5-28. Case 14 simulation result.

It was confirmed that once the MSS capacitors were switched in and out, they were prohibited from switching back in (within the time specified by input parameter @Tout).

Various combinations of deadband control, non-linear slope, and slow susceptance supplemental controls were attempted for dynamic simulations. Warnings and control disable actions were observed during initialization. Therefore, it has been confirmed that no combinations of these three supplemental controls can be implemented.

Case 14 was repeated with revised epcl code for the SVC Model to allow MSS switching of an inductor.

/********************/
/* MSS Logic Parm. */
/********************/

@Bics = 40.0 /* Larger threshold for switching MSSs */
@Bscs = 20.0 /* Smaller threshold for switching MSSs */
@Blis = -20.0 /* Larger threshold for switching MSSs */
@Bsis = -40.0 /* Smaller threshold for switching MSSs */
@Tmssbrk = 0.10 /* Time for MSS breaker to operate - typically ignore */
@tdelay1 = 0.50 /* Time delay for larger threshold */
@tdelay2 = 3.0 /* Time delay for smaller threshold (should be much larger than tdelay1) */
@Tout = 300.0 /* Time cap. bank should be out before switching back in */
Data from log file depicting the time when MSSs were switched in and out in the simulation:

- **MSC 1 AT SVC SWITCHED IN AT TIME:** 5.283582
- **MSC 2 AT SVC SWITCHED IN AT TIME:** 10.810758
- **MSC 3 AT SVC SWITCHED IN AT TIME:** 23.372885
- **MSC 1 AT SVC SWITCHED OUT AT TIME:** 42.02079
- **MSC 2 AT SVC SWITCHED OUT AT TIME:** 42.860786
- **MSC 3 AT SVC SWITCHED OUT AT TIME:** 43.919182
- **MSR 4 AT SVC SWITCHED IN AT TIME:** 60.605698
- **MSCs AT SVC ARE ALL OUT-OF-SERVICE OR NO MSRs TO SWITCH IN.
- **MSR 4 AT SVC SWITCHED OUT AT TIME:** 86.182686

Based on the simulation plot in Figure A-32, it was confirmed that both MSS capacitors and reactors were switched in and out as defined by the SVC model input parameters.

**Figure A-32. Case 14 simulation result with Inductor switching.**
**Case 15 – Step Change and Vary Firing Transport Delay (T2)**

Case 15 demonstrates the generic SVC model's response to a 2% step change (increase) at 1 second in the simulation with the valve firing transport delay increased.

- T2 increased from 0.01 to 0.05

The result was then compared to Case 6 in Figure A-33 and Figure A-34.

---

**Figure A-33. Case 15 simulation result**

**Figure A-34. Case 15 simulation result**
Case 16 – Power Oscillation Damping (POD) Control
An example of this test was shown in the main text of the report – see Figure 2-4.
<table>
<thead>
<tr>
<th>Case 12a</th>
<th>Case 12b</th>
<th>Case 3</th>
<th>w/deadband</th>
<th>w/out</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Units</td>
<td>Case 1</td>
<td>case 1b</td>
<td>Case 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>deadband</td>
<td>Case 13</td>
<td>Case 13_r1</td>
</tr>
</tbody>
</table>

### Input Parameter Description

<table>
<thead>
<tr>
<th>Parameter Description</th>
<th>Case 1</th>
<th>case 1b</th>
<th>Case 2</th>
<th>Case 3</th>
<th>w/deadband</th>
<th>w/out</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. cap. limit during undervoltage strategy (assumed filter size) @ UVSBmax pu (100 MVA)</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
</tr>
<tr>
<td>Under voltage setting 1 @ UV1 pu</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Over voltage trip time 2 @ OVtm2 sec</td>
<td>0.25</td>
<td>0.25</td>
<td>0.25</td>
<td>0.25</td>
<td>0.25</td>
<td>0.25</td>
</tr>
<tr>
<td>id of MSSs @ mscid2</td>
<td>“c2”</td>
<td>“c2”</td>
<td>“c2”</td>
<td>“c2”</td>
<td>“c2”</td>
<td>“c2”</td>
</tr>
<tr>
<td>id of MSSs @ mscid3</td>
<td>“c3”</td>
<td>“c3”</td>
<td>“c3”</td>
<td>“c3”</td>
<td>“c3”</td>
<td>“c3”</td>
</tr>
<tr>
<td>0 - no MSS switching; 1 - MSS switching on Q (MVAr) @ flag</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0 - linear droop; 1 - non-linear droop (piecewise)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Slope/droop @ CONT_X</td>
<td>0.1</td>
<td>0.02</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>Lower voltage break-point for non-linear</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slope/droop @ CONT_Vlow</td>
<td>0.95</td>
<td>0.95</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>Voltage measurement lag time constant @ CONT_Tb1 sec</td>
<td>0.01</td>
<td>0.01</td>
<td>0.01</td>
<td>0.01</td>
<td>0.01</td>
<td>0.01</td>
</tr>
<tr>
<td>Integral gain @ CONT_Kiv</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
</tr>
<tr>
<td>x</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rating) @ CONT_Bshrt pu (100 MVA)</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
</tr>
<tr>
<td>Min. susceptance of SVC @ CONT_Bmin pu</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Duration of short-term rating @ CONT_Tshort sec</td>
<td>3.33</td>
<td>3.33</td>
<td>3.33</td>
<td>3.33</td>
<td>3.33</td>
<td>3.33</td>
</tr>
<tr>
<td>Proportional gain of slow susceptance control @ CONT_Kp</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>Max. output of slow susceptance control @ CONT_Vrm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Steady-state Voltage deadband; SVC is inactive</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smaller threshold for switching MSSs @ Bin</td>
<td>2 Mvar</td>
<td>707</td>
<td>707</td>
<td>707</td>
<td>707</td>
<td>707</td>
</tr>
<tr>
<td>Larger threshold for switching MSSs @ Bout</td>
<td>-40 Mvar</td>
<td>-40</td>
<td>-40</td>
<td>-40</td>
<td>-40</td>
<td>-40</td>
</tr>
<tr>
<td>Larger than tdelay1) @ tdelay2 sec</td>
<td>6.66</td>
<td>6.66</td>
<td>3.6</td>
<td>3.6</td>
<td>3.6</td>
<td>3.6</td>
</tr>
</tbody>
</table>

Table A.2 - Model Parameter Input Parameters for Test Cases
FOR REFERENCE ONLY - DYNAMIC DATA FILE (dyd) FOR THE TEST CASE

#
# DYNAMICS DATA CREATED FOR TESTING SVC MODEL -- FOR WECC SVC MODELING TASK FORCE -- June 2008
#
# DAN SULLIVAN, Mitsubishi Electric Power Products, Inc. (MEPP)
# POUYAN POURBEIK, Electric Power Research Institute (EPRI)
#
# sinval 7 *BUS-7 *230.00 97 *: *# *mva=100.00000 *"Generic_SVC.c1 p" 3.00000 *"comm" 0.00000 /
# "commm" 0.00000 *"Theta_Th" 0.00000 *"Theta_T" 0.00000 *"Vp" 0.00000 *"Wip" 0.00000 *"Wt" 0.00000 *"delay_g" 0.00000 /
# T_Im 0.00000 *"Vref_p" 1.00000 *"V_ref_p" 1.00000 *"T_ref" 1.00000 *"T_ref" 1.00000 *"T_ref" 1.00000 /
# delay_c 0.00000 "B_cap" 0.00000 "C_cap" 0.00000 "wref_lw" 0.00000 "wref_hg" 0.00000 "accel" 0.00000 /
# motor 2 *BUS-2 *250.00 01 *: *# *mva=0.00000 0.400000 3.60000 170.0000 0.500000 0.600000 0.600000 2.00000 0.800000 30.0000 0.033330 0.600000 0.170000 0.0 10.0000 0.800000 /
# motor 4 *BUS-4 *115.00 01 *: *# *mva=0.00000 0.400000 3.50000 0.170000 0.000000 0.000000 0.000000 2.00000 0.600000 30.0000 0.033330 0.600000 0.170000 0.0 10.0000 0.600000 /
# genset 1 *BUS-1 *230.00 01 *: *# *mva=156.60000 4.800000 0.000000 0.4100 0.070000 /
# 6.5000 0.000000 2.1400 2.0200 0.2400 0.9000 0.23000 /
# 0.1900 0.1000 0.40000 0.00000 0.000000 0.000000 0.000000 /
# excit 1 *BUS-1 *230.00 01 *: *# *mva=0.020000 3.1500 3.1500 0.010000 1.000000 0.870000 1.000000 0.0 1.000000 0.8700000 /
# 0.0 6.6000 0.0 0.000000 0.0 0.000000 /
# generator 6 *BUS-6 *115.00 91 *: *# *mva=156.60000 4.800000 0.000000 0.4100 0.070000 /
# 6.50000 0.00000 2.1400 2.0200 0.2400 0.9000 0.23000 /
# 0.1900 0.1000 0.40000 0.00000 0.000000 0.000000 0.000000 /
# excit 6 *BUS-6 *115.00 91 *: *# *mva=0.020000 3.1500 3.1500 0.010000 1.000000 0.870000 1.000000 0.0 1.000000 0.8700000 /
# 0.0 6.6000 0.0 0.000000 0.0 0.000000 /
# VMEM 1 *BUS-1 *230.00 01 *: *# *mva=0.00000


**MODELING THE SVC AT THE TRANSMISSION LEVEL**

There is often a discussion as it pertains to SVCs as to whether the device should be modeled at the transmission level or if the unit’s transformer should be explicitly modeled and the SVC branches modeled explicitly at low voltage bus of the unit transformer.

This issue has been discussed and documented in the literature (e.g., [7]). None-the-less, it is felt that a brief summary of the subject is pertinent for clarity.

It should be noted that a typical specification of an SVC installation by a utility will specify the required SVC range at the transmission level bus (the high voltage side of the SVC coupling transformer – bus 1 in Figure B-1). Large SVC applications are primarily for transmission system voltage support, thus the equipment specification will be for require reactive support at the transmission voltage level. Furthermore, a typical specification will identify the range of steady-state voltages for which the full reactive capability of the SVC should be available continuously (e.g., from 0.9 to 1.1 pu voltage).

Furthermore, a typical SVC control system will actually control the unit’s susceptance (B) as measured on the high voltage side of the coupling transformer.

Thus, vendors will optimize and design the combination of the SVC branches (TCR/TSC) and the coupling transformer to ensure that the effective SVC range at the transmission system voltage is as required and specified. In addition, the equipment is designed to sustain the higher voltage that will inherently occur at the secondary of the coupling transformer over the required continuous operating range of the SVC. Thus, the secondary voltage limitation control, the TCR and TSC current limiters will not typically come into play for momentary transients (e.g., faults and power swings) or during steady-state operation in the normal continuous range. As such, there is no value in modeling the coupling transformer explicitly and going to the complication of calculating the branch values at the secondary voltage level. Moreover, when performing studies to specify a potential SVC application, one can only truly assess what is needed at the transmission level – the sizing of the branches and coupling transformer are part of the optimization process of actual equipment design, best done by the equipment vendor.

As a simple exercise, consider the following example. Consider the two equivalent SVC models in Figure B-2. On the left hand side we have the model with the transformer explicitly modeled. In this case, the device total susceptance as seen at the high-voltage bus (Bus 1) is:
Thus, the two models are identical at the transmission level. Figure B-3 shows
the VI characteristics of both models as seen at bus 1 (high voltage side). That
is, \( I = V \times B \). This is further illustrated in Figure B-4 and B-5, which show the two
cases simulated in GE PSLF™.

![Figure B-1: SVC and coupling transformer.](image-url)
\[ jX_t = 0.1 \text{pu} \]

\[ jB_{svc_{\text{max}}} = 1.667 \]
\[ jB_{svc_{\text{min}}} = -1.11 \]

Figure B-2: SVC modeled with and without the coupling transformer.

\[ jB_{svc_{\text{max}}} = 2.0 \]
\[ jB_{svc_{\text{min}}} = -1.0 \]

Figure B-3: SVC VI characteristic from 0 to 1 pu voltage (ideal case, not showing protection and under/overvoltage strategies).
Figure B-4: High Side Model – Bmax = 2.0. Delivered Q at 1 pu voltage at 230 kV is 200 MVAr (see top figure; note line between bus 7, where SVC is located, and bus 3 is negligible, it has only been added to separate the buses)
Figure B-5: Low Side Model – Bmax = 1.6667. Delivered Q at 1 pu voltage at 230 kV is 200 MVAr (see top figure; note 10%, on 100 MVA, transformer modeled from bus 7, where SVC is located at).