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Generic Static Var System Models for the Western Electricity Coordinating Council

Prepared by WECC Static Var Compensator Task Force, of the Modeling and Validation Working Group

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Sincere gratitude is due to the software vendors who have adopted models that were developed and implemented them in their standard model libraries, namely GE and Siemens PTI. Of course, in the process GE and Siemens PTI thus significantly contributed to the whole effort. We look forward to other software vendors adopting these models, such as PowerTech Labs and PowerWorld.

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1. INTRODUCTION

This is a report of the work of the WECC Static Var Compensator (SVC) Task Force (TF) of the WECC Modeling and Validation Working Group.

The mission statement of the SVCTF is:

Invest best efforts to accomplish the following:

- Improve power flow and dynamic representation of Static Var Systems (SVS) in positive-sequence simulation programs with a focus on generic, non-proprietary power flow and dynamic models. An SVS is defined as a combination of discretely and continuously switched Var sources that are operated in a coordinated fashion by an automated control system. This includes SVCs and STATCOMs.
- The models should be suitable for typical transmission planning studies. Power flow models should be suitable for both contingency and post-transient analyses. Dynamic models should be valid for phenomena occurring in a timeframe ranging from a few cycles to many minutes, with dynamics in the range of 0.1 to 10 Hz, and simulated with a time step no smaller than ¼ cycle.
- To develop a modeling guideline document.
- To collaborate with manufacturers and other stakeholders, IEEE, CIGRE, EPRI, etc.

The goal of the SVCTF is to develop more comprehensive models to better represent both existing and future SVS installations. In all modeling efforts, there is always a balance to be achieved between detail and flexibility. The SVCTF is developing a generic, non-proprietary model that is flexible enough for use in modeling existing facilities and newly proposed SVS. It is fully realized that it would not be possible for such a model to cater to every conceivable configuration of equipment and control strategy. Occasionally, some additional user-written supplemental controls may be needed to augment the models presented here.

More specifically the SVCTF is developing:

1. A generic SVS model for a thyristor-controlled reactor (TCR)-based SVC to be coordinated with Mechanically Switched Shunt (MSS) devices.
2. A generic SVS model for a TSC/TSR-only based SVC coordinated with MSSs.
3. A generic SVS model for a voltage source converter (VSC) based STATCOM coordinated with MSSs.
4. Enhanced power flow models that at minimum will capture the:
   a. Coordinated MSS switching logic based on susceptance.
   b. Slow-susceptance control feature of SVCs.

c. Slope (droop or current compensation).

5. A directly associated dynamic SVS model with a switchable/controllable shunt model in power flow (rather than having to connect the dynamic model to a generator model).

To achieve the above goals, the following approach was taken:

Step 1 – develop a prototype dynamic model of the generic SVS (item 1 above) in GE PSLF™, as a user-written model, and verify its performance.

Step 2 – run some simulation tests on the model.

Step 3 – release the code publicly to allow its implementation as a standard model library item in GE PSLF™,[1] Siemens PTI PSS/E™,[2] and any other software tools. In parallel, extend the model to cover items 2 and 3 above (i.e., TSC/TSR-based and STATCOM-based SVS).

Step 4 – in parallel to all of the above, implement changes to develop a power flow algorithm to be implemented in GE PSLF™, Siemens PTI PSS/E™, and any other software platform that wishes to adopt it.

Step 5 – document the work.

The model developed here is heavily based on the documents listed in Section 5: References as [1], [2], [3], and [9]. The project was started with the code provided by Tucson Electric Power and Pacific Gas and Electric during meetings of the WECC SVCTF (which is code developed by ABB Inc.). This code has been modified to incorporate a few extra features discussed and presented during the SVCTF meetings [4], [5], and [6] in order to make the model more generic. One additional pertinent reference is [7].

The finalized code for the TSC/TCR-based SVC has been tested and approved, and released and thus implemented in the GE and Siemens PTI programs, and may be adopted by other vendors too.

The code associated with the document [9] has been generously provided to the SVCTF by ABB and thus passed along to GE and Siemens PTI (and other SVCTF members) to start the process of implementing it as the generic STATCOM dynamic model. The model was approved at the last SVCTF meeting.

The document [10] was sent to the SVCTF by Siemens PTI as the first proposal for the TSC/TSR SVS dynamic model.

This document is a detailed account of the first and completed model, the TCR-based SVS, which is referred to as the *svsmo1* model.

[1] Positive Sequence Load Flow/GE PSLF Software
[2] Siemens/Power Technologies International: Power System Simulator for Engineering

2. THE GENERIC SVS MODELS

2.1 The Time-Domain Dynamic Models

Some Basic Assumptions

The intended use of the models presented here are for power system simulation studies in positive sequence stability programs. Furthermore, we are concerned with phenomena that:

- o range typically between a few tens of milliseconds to tens of seconds
- o have frequencies of 0.1 Hz to 3 Hz (inter-area to local modes of electromechanical oscillation)
- o affect (occasionally) controller dynamics (i.e., stability of the voltage control loop) that may be in the 10 Hz or so range

Also, in this document the following assumptions are made:

- o Susceptance, reactive currents, and reactive power are defined to be positive if they are capacitive (being injected from the shunt device into the power system) and negative if they are inductive (being absorbed by the shunt device from the system).
- o The models developed here are intended for power system planning studies and represent the general dynamic behavior of SVS. The models do not represent the specific details of actual controls.

The TCR-based SVS (SVSMO1)

This section documents the dynamic (time domain) generic model for an SVS that is comprised of a thyristor-based SVC potentially coupled with coordinated mechanically switched shunts[3] (MSSs). Furthermore, it is assumed that at least one TCR branch exists. For the purpose of positive sequence simulations, the SVC can be modeled as a smoothly and continuously controllable susceptance throughout its entire range.

In developing the SVC model, the SVCTF made the following broad but reasonable assumptions:

1. The pertinent key control loops that should be modeled are:
    a. The voltage regulator
    b. The coordinated switching logic for MSSs
    c. The slow-susceptance regulator, if any
    d. Deadband control, if any

[3] That is, allowing for either switched shunt capacitors or inductors.

e. SVC slope/droop

f. SVC limits, over- and under-voltage strategy and voltage trip set points

g. Any short-term rating capability

2. What is not pertinent for modeling are:

a. TCR and TSC current limits – for large transmission SVCs, the equipment will typically be specified to be able to deliver full reactive capability throughout the range of steady-state continuous primary voltage (system voltage), typically 0.9 pu to 1.10 pu. It is not expected that these current limiting devices will come into play for power system studies.

b. Secondary Voltage Limitation – the secondary voltage on the low voltage side of the SVC step-up transformer may be limited by constraining the capacitive output of the SVC. Once again, the equipment will be typically specified to be able to deliver full reactive capability throughout the range of steady-state continuous primary voltage (system voltage), typically 0.9 pu to 1.10 pu. It is not expected that this limiting control will come into play for power system studies. This is not necessarily true for a STATCOM due to the more tightly controlled current limits and should typically be modeled for STATCOMs where necessary.

c. Gain scheduler – this is typically some form of adaptive controller that adapts the open loop gain of the SVC to the particular system conditions. For example, if the system conditions become weak and result in the initiation of oscillations in the SVC voltage control loop (due to high open loop gain for the given condition), the gain scheduler will sense this and reduce the voltage regulator gain until the oscillations are suppressed.

d. This constitutes too much detail for typical power system studies. The user should choose an appropriate gain to ensure stable closed-loop operation for the given network conditions being studied. Most studies look at N-1, N-1-1 and N-2 conditions. Such conditions do not typically lead to the extreme changes in network short circuit level that would initiate operation of the gain scheduler.

e. Other auxiliary controls and details (cooling system controls, etc.) that have little to no bearing on system dynamic performance studies.

The final generic dynamic SVS model is shown below.

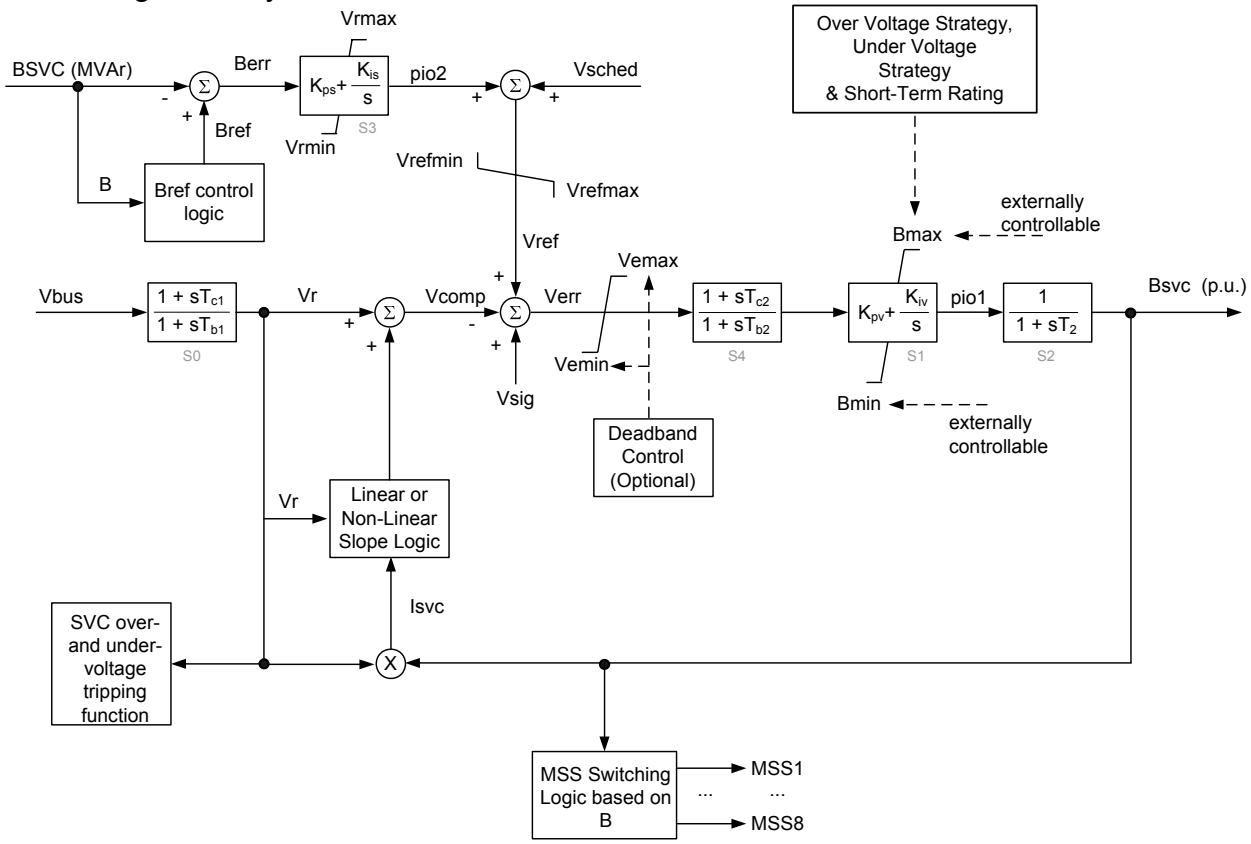

Figure 2-1: The generic SVSMO1 model of an SVC-based SVS, assuming an SVC with at least one TCR branch.

Figure 2-2 shows the VI characteristic of the SVC component of the SVSMO1 model. This figure is illustrative and is not intended to represent the actual VI characteristic of any device. The full parameter list for the model is provided in Appendix D.

The prominent features of the model are:

- o Proportional-Integral Primary Voltage Regulation Loop: This is the heart of the SVC. Kpv and Kiv are the proportional and integral gain of the control loop. (Note: to be even more generic one could add an optional additional derivative gain; however, including derivative control is quite rare for large transmission SVCs). A word of caution for the user. The proportional gain of the proportional and integral (PI) regulator typically has a negative impact on any oscillations throughout the frequency range, which will have a negative effect on higher frequency oscillations whereas the gain of an integrating regulator will rapidly reduce with increasing frequency. The reason that a PID regulator[4] is almost never used in flexible AC transmission systems (FACTS) devices is the rapid gain increase with

[4] Proportional-integral-derivative regulator.

frequency. This model only provides the ability to implement PI and I regulators.[5] Even in this case the user should be cautious since positive sequence programs are not able to model network phenomena higher than about two or three Hz. What may appear as an attractive PI control in stability analysis using a positive sequence simulation program, may have adverse effects on oscillation modes outside the simulation programs frequency range in practice. This requires knowledge from the user to be able to have the necessary judgment to provide proper tuning. Also, in special cases more detailed three-phase equipment level modeling and analysis may be needed, and should be coordinated with the equipment vendor. Note: in this model we assume that the integral gain is always non-zero.

WARNING – *the user must be aware that if PI control is used in this stability-type model, excessive proportional gain may lead to undesired reduction in damping of network phenomena in higher frequency bands that are not modeled in stability programs (i.e., above the two–to-three Hz range).*

- Lead/Lag Block for Voltage Measurement: The block with time constants Tc1/Tb1 represents the voltage measurement process.
- Lead/Lag Block for Transient Gain Reduction: The block with time constants Tc2/Tb2 can be used to introduce transient gain reduction or simply to experiment with the impact of SVC response on damping through phase lead compensation. Typically, it is not used.
- Slow Susceptance Regulator: The PI regulator Kps/Kis is the slow susceptance regulator that slowly biases the SVC reference voltage between the values of vrefmax and vrefmin to maintain the steady-state output of the SVC within the bandwidth of Bscs and Bsis. The Bref control logic (see Figure 2-1) is as follows:

  If (B < Bsis) then Bref = Bsis + eps

  If (B > Bscs) then Bref = Bscs – eps

  Otherwise Bref = B

  Where *eps* is a small delta (e.g., 0.5 Mvar) to ensure that the slow susceptance regulator does not interact with the MSS switching, since typically the first (larger delay) switching point of the MSSs is set to the same band as the slow susceptance regulator. Note: in the dynamics model the output of this regulator, *pio2*, is always initialized to zero.
- Over/Under-Voltage Control Strategy:

  The following under-voltage strategy is implemented:

[5] Integral regulator.

- If the SVC bus voltage is less than a given value (parameter UV1[6]) the SVC susceptance will be limited to a set value (parameter UVSBmax), which may typically be the fixed filter banks or zero output.
    i. If the voltage returns in less than a set time delay (parameter UVtm1), then the SVC will continue normal operation.
    ii. If the voltage returns in a timeframe longer than UVtm1 (typically, seconds) then there will be a small delay associated with the PLL to re-synchronize the SVC so that it may resumes normal operation. This delay (typically around 100 to 150 ms) is represented by the parameter PLLdelay.
- If the voltage falls below a more severe voltage level (parameter UV2), e.g. UV2 = 0.3 pu, then the SVC is forced to its inductive limit to prevent an overvoltage when the system voltage is restored.

During overvoltage conditions where the SVC bus voltage exceeds a given level (parameter OV1), the SVC output is forced to its inductive limit immediately. This is the overvoltage strategy.

- Over/Under-Voltage Protection: To protect the SVC equipment from prolonged overvoltage or undervoltage conditions, the SVC will trip after a given definite time delay. The model includes features that attempt to emulate this behavior. The logic is as follows: If the SVC terminal voltage is below UVT for more than UVtm2 seconds, the SVC model status is set to zero (SVC trips). If the terminal voltage exceeds OV1 (or OV2) for more than OVtm1 (or OVtm2) seconds, the SVC will trip (OV1 is the same parameter used above in the over-voltage control strategy).
- Short-Term Rating: Short-term rating is modeled (that is, the SVC output can exceed its continuous rating up to a given amount for a short time period). This is modeled by the parameters Bshrt and Tshrt. That is, the SVC capacitive output can go to Bshrt for up to Tshrt seconds.
- Optional Deadband Control: This is an optional deadband controller. The deadband control, slow susceptance regulator, and non-linear droop are all intended for the same purpose – maintaining the SVC at a low steady-state output when the system voltage is within a given bandwidth. However, these three control strategies achieve this in quite different ways.

  For stable and suitable control response in simulations, the use of any combination of deadband control, slow-susceptance regulation, and non-linear slope/droop is **highly discouraged**. Only one of the three should be

[6] For example, UV1 = 0.6 pu – this is a tunable parameter and the setting is based on the studies and the need of the particular system, e.g., see [1].

used. The model checks for this conditions during initialization and does not allow the use of combinations of these controls[7].

The deadband controller, as implemented in the model, is not necessarily meant to represent the exact control strategy, but rather to be a generic representation of deadband control. The approach presented here ensures that the model initializes properly and within the deadband limits when one goes from powerflow to dynamics. The reference voltage of the SVC is taken to be the scheduled voltage at the bus from powerflow. Vdbd1 defines the deadband around this voltage.

If upon model initialization the bus voltage is found to be outside this range (i.e., outside Vschedule + Vdbd1 to Vschedule – Vdbd1) then the user is warned and Vref is set to the actual solved bus voltage – in order to prevent initialization problems with the model.

Figure 2-6 below explains the deadband logic modeled. In the figure when it is said that the SVC is “locked at present VAr output”, this means that the voltage error (Verr) is force to zero and the output of the SVC remains at its current state until voltage moves outside the deadband again. The deadband control is modeled by the three parameters Vdbd1, Vdbd2, and Tdbd.

- Linear and Non-Linear Slope/Droop:

  If the parameter flag2 is set to 0 then a standard linear droop of Xc1 is assumed, as is typical in most designs. Droop is the ratio of voltage change to current change over the defined control range of the device. For example, if a 3% voltage change is allowed across the entire control range of an SVC, and the SVC is rated +200/-100 Mvar and we assume a system MVA base of 100 MVA, then the slope is Xc = 0.03/3 = 0.01 pu on 100 MVA base.

  Alternatively, by setting flag2 to 1, one can use a three piece piecewise linear droop setting. This can be used to make the SVC non-responsive in a given bandwidth, similar to deadband control.

  The logic for this is as follows (see Figure 2-1 and Figure 2-8):

[7] Note: in practice, with careful study and design, it made be possible to use a combination of these controls (e.g. dead-band and slow-susceptance control).

```
if ( flag2 = 0 )
        Xc = Xc1
else
        if ( Vr >= Vup )
                Xc = Xc1
        elseif ( (Vr < Vup) and (Vr > Vlow) )
                Xc = Xc2
        else
                Xc = Xc3
        end
end
y = Xc*Isvc = Xc*V*B
```

This control is more susceptible to limit cycling if not properly tuned. Note: upon initialization, the model checks to make sure the initial SVC output is zero (0) Mvar and that the initial bus voltage is in the middle of the range (i.e., (Vup + Vlow)/2, see Figure 2-8). This is a necessary condition for proper initialization.

- MSS Logic: Detailed MSS logic is implemented that allows for automated MSS switching based on SVC VAr output. Two thresholds (typically, one for fast switching and one for slow switching) are implemented with different delays on switching (parameters Bscs, Blcs, Bsis, Blis, Tdelay1, Tdelay2). The MSS discharge time can also be set (i.e., time the MSS must be switched out before it can be switched back in; this applies only to shunt capacitors – parameter Tout). The MSS breaker delay is also modeled (parameter Tmssbrk). Note: if used, MSS switching must be properly coordinated with the slow-susceptance regulator. Typically, to avoid excessive MSS switching, the slow-susceptance regulator time constant is chosen such that it acts first to bring the SVC to within the first threshold. If it is unable to achieve this, then the MSSs switch. The delay time on the first (smaller and slower) threshold for MSS switching is chosen to be significantly longer than the slow-susceptance time constant. Also, the slow-susceptance time constant is much longer than the primary voltage regulator loop response time. Figure 2-9 demonstrates in a flow chart format the MSS switching logic. Figure 2-7 shows a simple illustration of this logic. Reference [8] reports an actual field implementation of this type of MSS switching logic, for a case with only mechanically switched capacitors.
- The Lag Block (T2): This represents the delay in the firing circuit of the SVC. Although in the past this has been modeled as a pure delay (e^{-st}) or a combination of a pure delay and lag block [7], here for the sake of simplicity the SVCTF has chosen to use a single lag block. It should be noted that the susceptance feedback to the slope calculation is taken as the actual susceptance after the firing delay. In reality this susceptance may actually be the susceptance command or a measured value. Such nuances are not particularly important for the purposes of the modeling work here that is focused on power system stability analysis.

- The SVC Susceptance Limits: The susceptance limits, parameters Bmax and Bmin, are externally controllable by the user through separately written user code. This has been provided for added flexibility in the case where a user may wish to model other functionality (e.g. emulate through user-written code the response of the secondary voltage limitation loop and TCR/TSC current limiters, and thus attempt to model the SVC transformer etc.). This is not recommended; for planning studies the model provided, and modeled at the transmission level, should be more than adequate (see Appendix B).
- Power Oscillation Damper (POD), and the Voltage-based MSS Devices: These have separate control loops so they are separate supplemental models.

  A separate supplemental damping controller can be connected to the main model at Vsig, as shown in Figure 2-1. Figure 2-3 shows the block diagram of an example damping controller.

  Figure 2-5 illustrates a case that was simulated with and without the generic POD applied at the Vsig input shown in Figure 2-1. The plot shows power oscillations on the remaining tie-line from bus 2 to 3 (in Figure A-1) when the second line is faulted and tripped. The generator models were tweaked to provide increased oscillations. The intent here is not to show how to tune a POD but simply that it works and can be applied to an SVC – more specifically the SVC model developed here. For more details on SVC POD tuning see references 17, 18 and 19 in Section 6.

  A separate stand alone model for switching shunt-devices based on voltage set points (see Figure 2-4) is provided in GE PSLF™ and Siemens PTI PSS™E. This model allows for switching the shunt in (or out) once the voltage falls below (or rises above) a certain value, for a given amount of time. It also models the discharge time required for a shunt capacitor (which can be set to either zero for reactors or to a small value for fast-discharge capacitors).

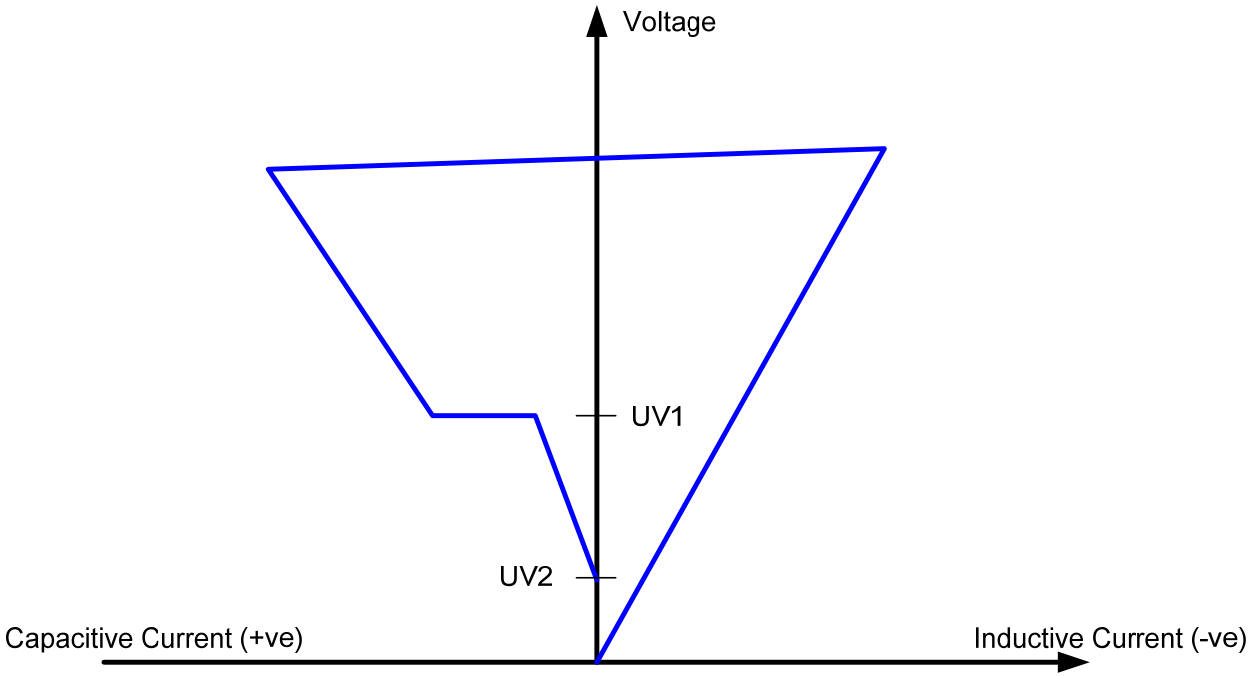

Figure 2-2: VI characteristic of an SVC.

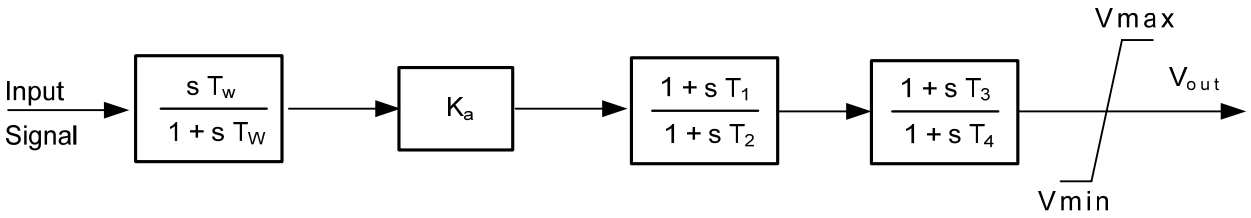

Figure 2-3: Generic Damping Controller

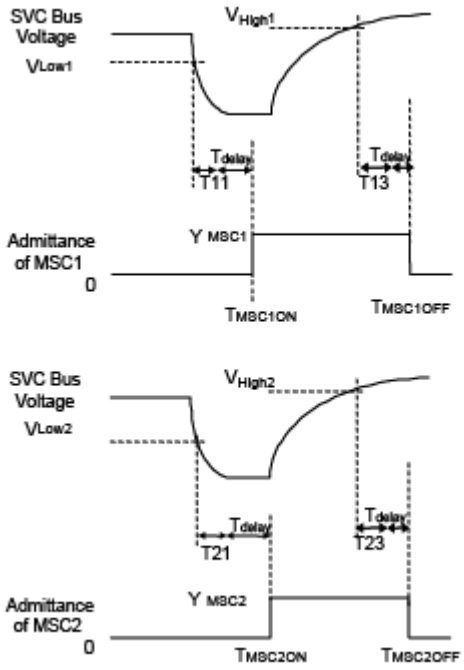

Figure 2-4: Voltage-Based MSS switching (reproduced from [11] IEEE© 2006)

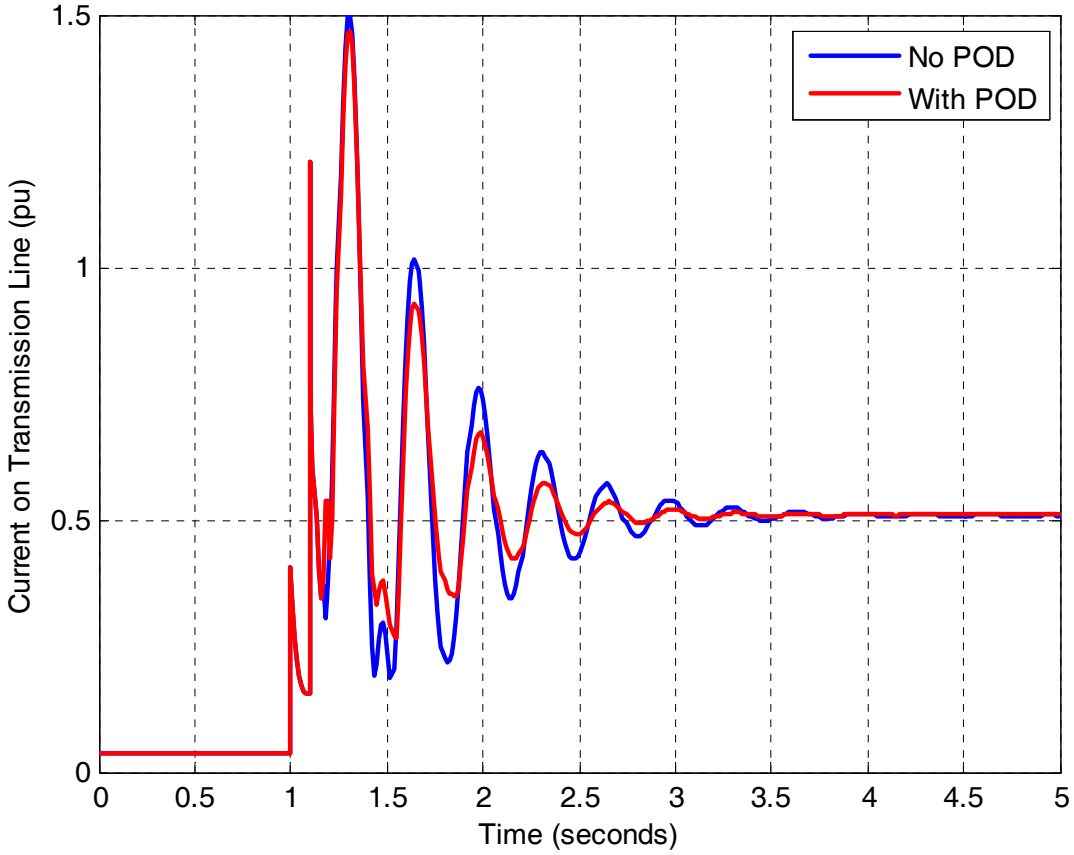

Figure 2-5: Illustration of the functioning of the POD.

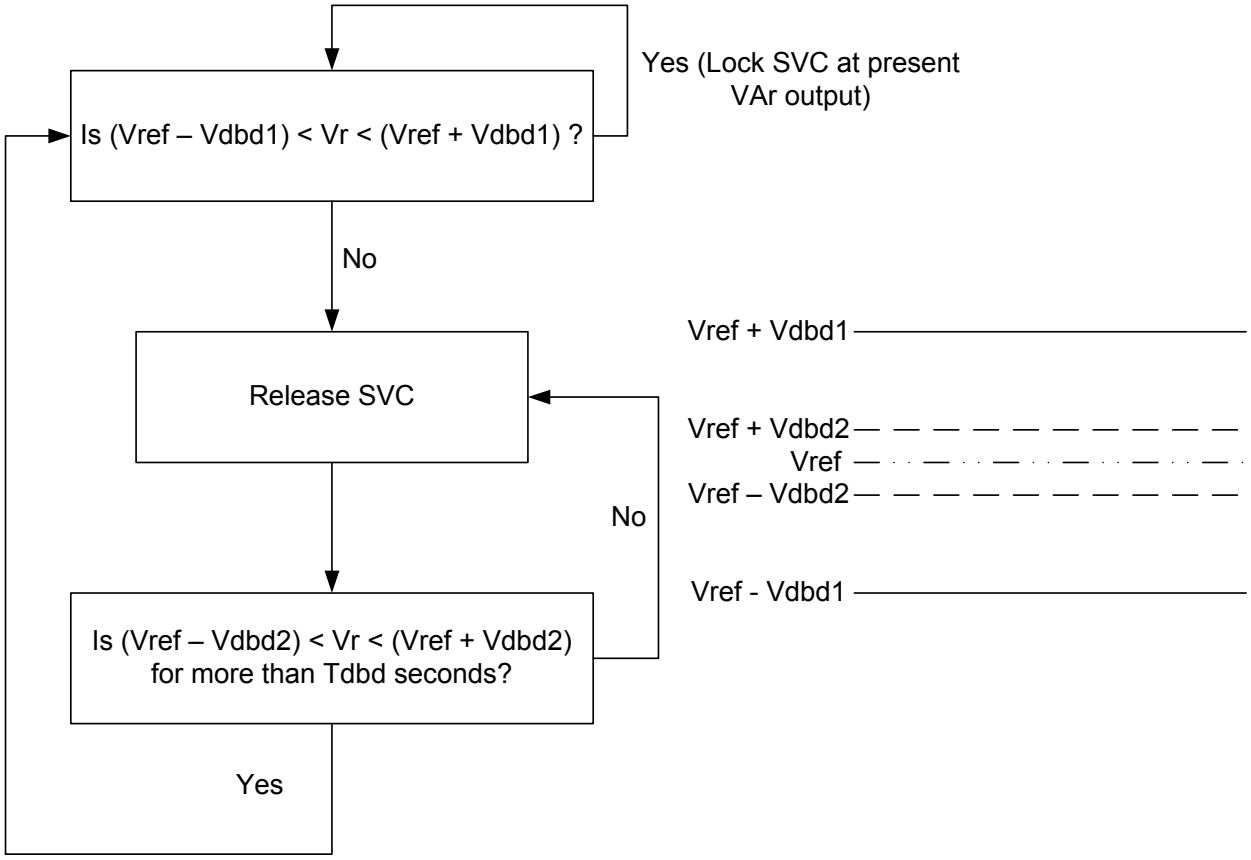

Figure 2-6: Deadband control logic.

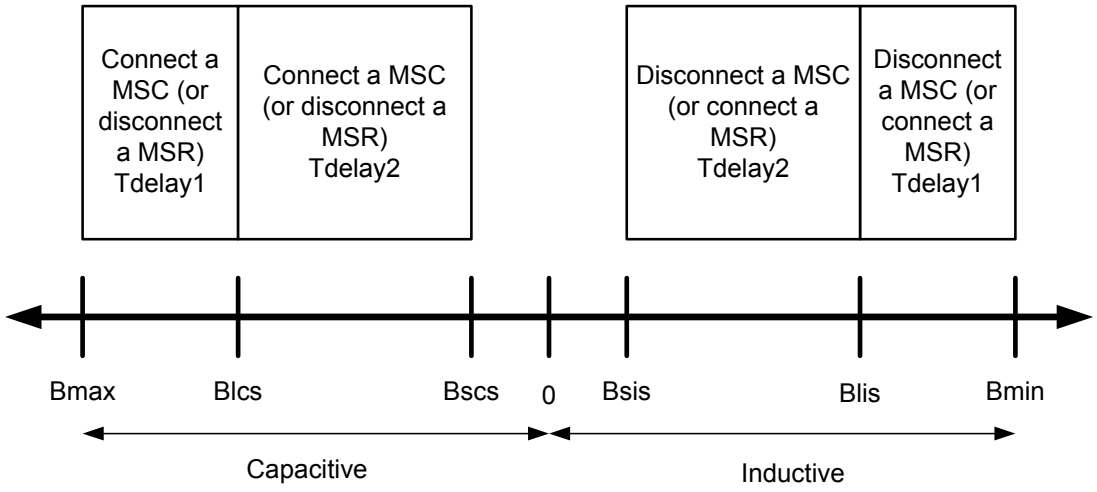

Figure 2-7: Settings for the MSS switching logic based on SVC susceptance.

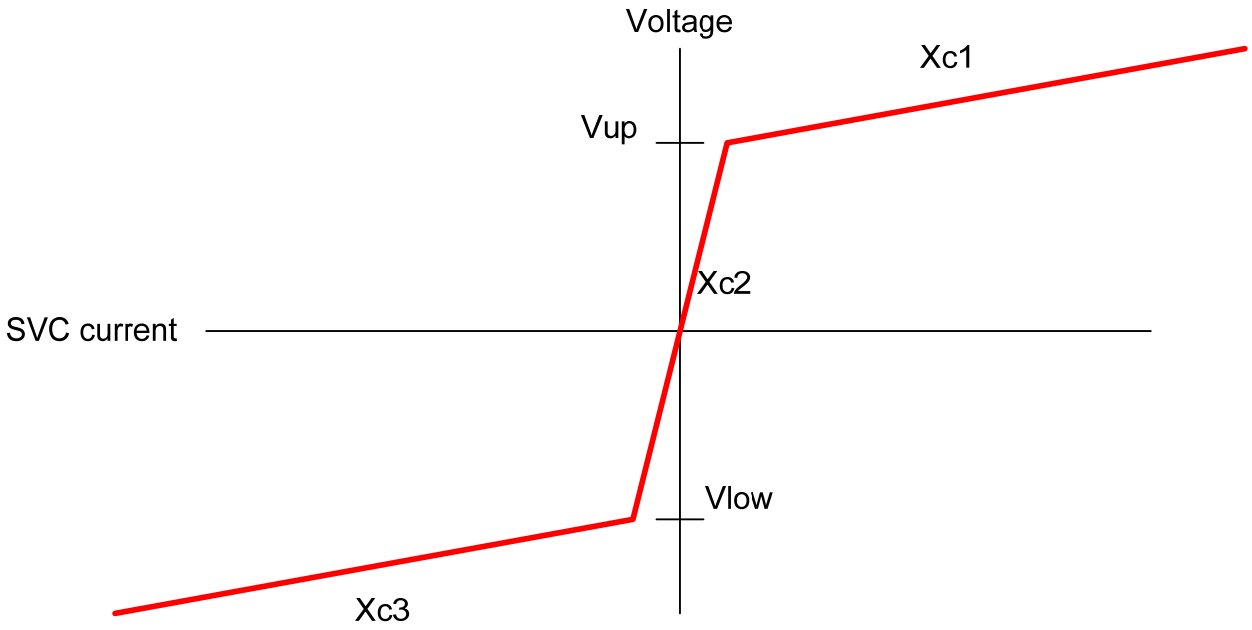

Figure 2-8: Non-linear droop

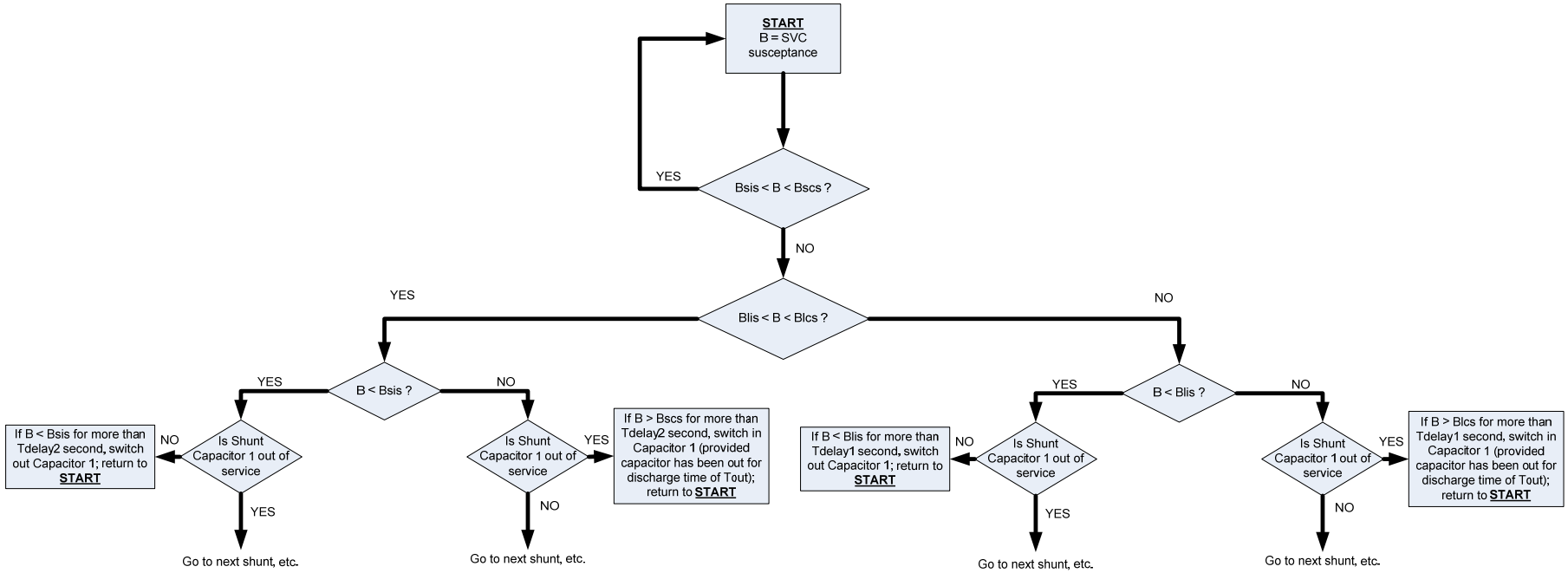

Figure 2-9: MSS switching logic

The TSC/TSR-based SVS (SVSMO2)

The majority of the functionality of SVSMO2 is identical to the SVSMO1 model. Thus, most of the parameters and discussion above are equally applicable to the SVSMO2 model. The full parameter list for the model is provided in Appendix D. The key difference is that the SVC component of the SVSMO2 consists of only thyristor switched capacitors and reactors, thus making its output discretely stepped. In contrast the SVSMO1 includes a thyristor controlled reactor which makes its output smoothly controllable. Figure 2-10 shows the SVSMO2 dynamic model. A comparison of Figure 2-1 and Figure 2-10 shows that the major difference is the presence of the “look-up table” block between the susceptance command and the SVC output. This block determines the unique combinations of the TSC/TSR branch elements and then determines the combination that is closest to the current susceptance command and effects that desired susceptance.

A simple example will demonstrate the functionality of the look-up table. The look-up table comprises of all combinations of the discrete TSC/TSR branches. For example, if an SVC has three branches;

5 Mvar TSC

10 Mvar TSC

-5 Mvar TSR

then all combinations (in ascending order) for these three branches are:

Combination	MVAr Output
001	-5
101	0
100	5
010	10
110	15

where we deliberately neglect combinations that lead to the same Mvar output. Thus, the possible outputs of this device are -5, 0, 5, 10 and 15 Mvars. Also, a small hysteresis is implemented to ensure that the device does not hunt between choices of combinations of branches.

The parameter list for the SVSMO2 is essentially the same as SVSMO1, with the addition of two mandatory parameters *dbe* and *dbb*. A deadband on the voltage error (*dbe*) and a hysteretic deadband on the switching point for going from one susceptance value to the next higher (or lower) value (*dbb*). These are shown in Figure 2-10. The software tool should internally calculate the look-up table based on user input of the number and size of TSC/TSR branches, which is typically entered in the powerflow tables.

The action of the hysteretic deadband (*dbb*) can be described by a diagram, as shown in Figure 2-11. If we are presently at the susceptance output of B1 on the SVC (e.g. from our previous example B1 = 5 Mvar, at 1 pu voltage), then as the susceptance command from the PI regulator changes (pio1) the output of the SVC stays the same until this command exceed the mid way point between B1 and the next discrete possible output point B2 (e.g. B2 = 10 Mvar from our example above) plus dbb. Thus, if dbb = 0.5 Mvar and B1 = 5 Mvar and B2 = 10 Mvar, then once the susceptance command goes above 5 + (10 – 5)/2 + 0.5 = 8 Mvar the SVC output goes immediately to B2 = 10 Mvar. However, on the way down there is a hysteretic behavior and the command must go below the mid-way point by dbb for it to go back to B1, i.e. it must go below 5 + (10 – 5)/2 – 0.5 = 7 Mvar. In this way by making the switching point hysteretic (i.e. direction dependant) any hunting between switching points is prevented. This is an emulation of the controls and is not intended to be an exact implementation of any specific control strategy.

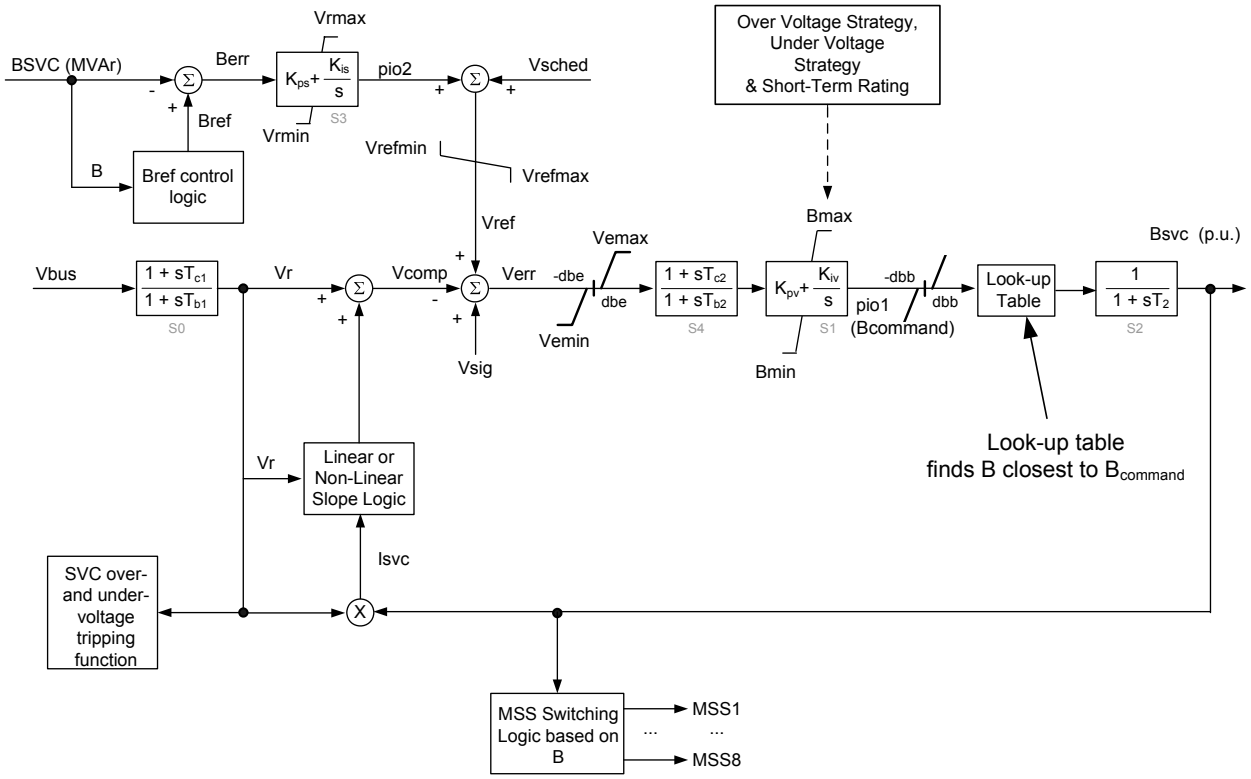

Figure 2-10: The generic SVSMO2 model of an SVC-based SVS, assuming an SVC with only TSC and TSR branches.

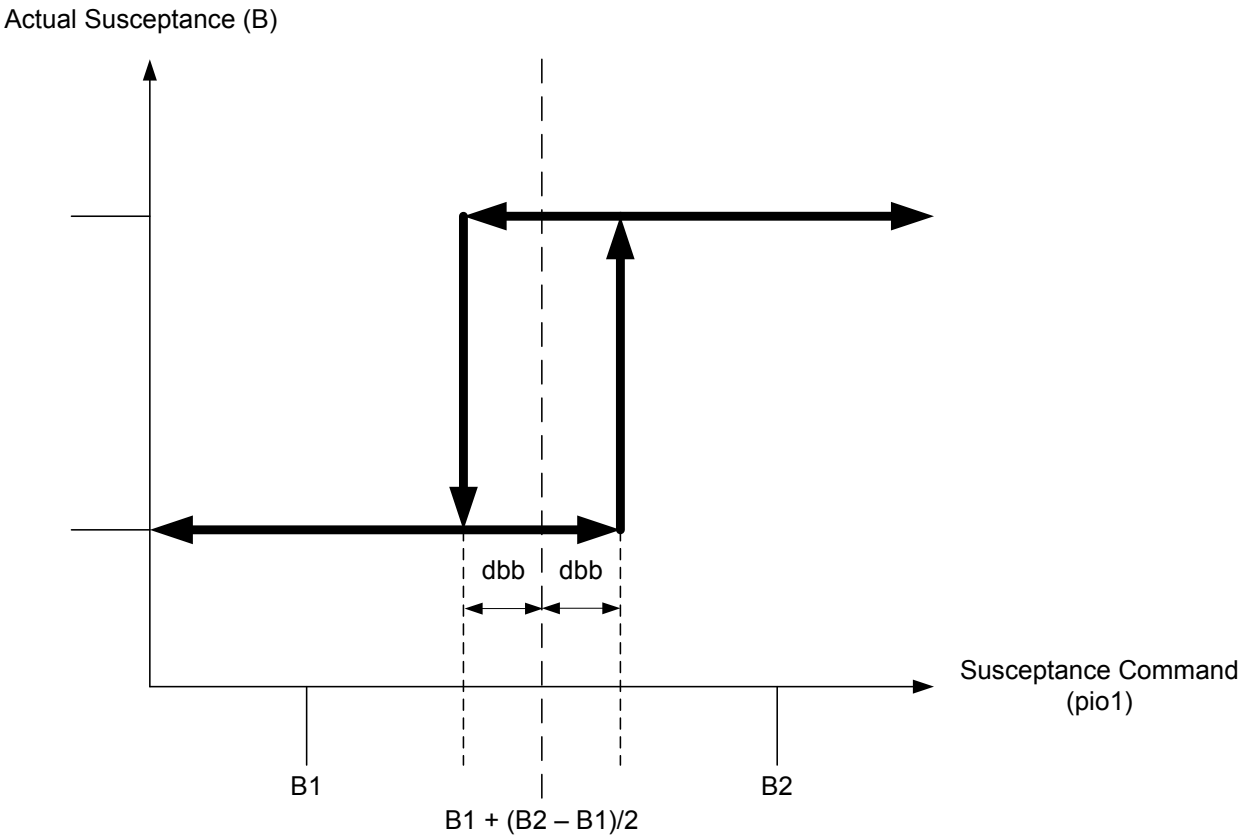

Figure 2-11: Switching from one susceptance level to the next.

The VSC-based SVS (SVSMO3)

Figure 2-12 shows the block diagram of the SVSMO3 model (based on [9], with some slight modifications). A perusal of this figure and that of SVSMO1 shows that the major difference between the two models is that SVSMO3 assumes a voltage source converter (VSC) based SVS. That is, the power electronic device in this case is a static compensator (STATCOM) which is an active device and at its reactive limit will act as a constant current source, rather than a constant susceptance. The VI characteristic of this device is as shown in Figure 2-13.

The similarities with the SVSMO1 model are the following:

1. The main PI voltage regulator loop (Kp/Ki).
2. The lead-lag blocks Tb1/Tc1 and Tb2/Tc2.
3. The firing control delay (lag time constant To).
4. The linear or non-linear slope (Xco, Xc1, Xc2, Xc3).

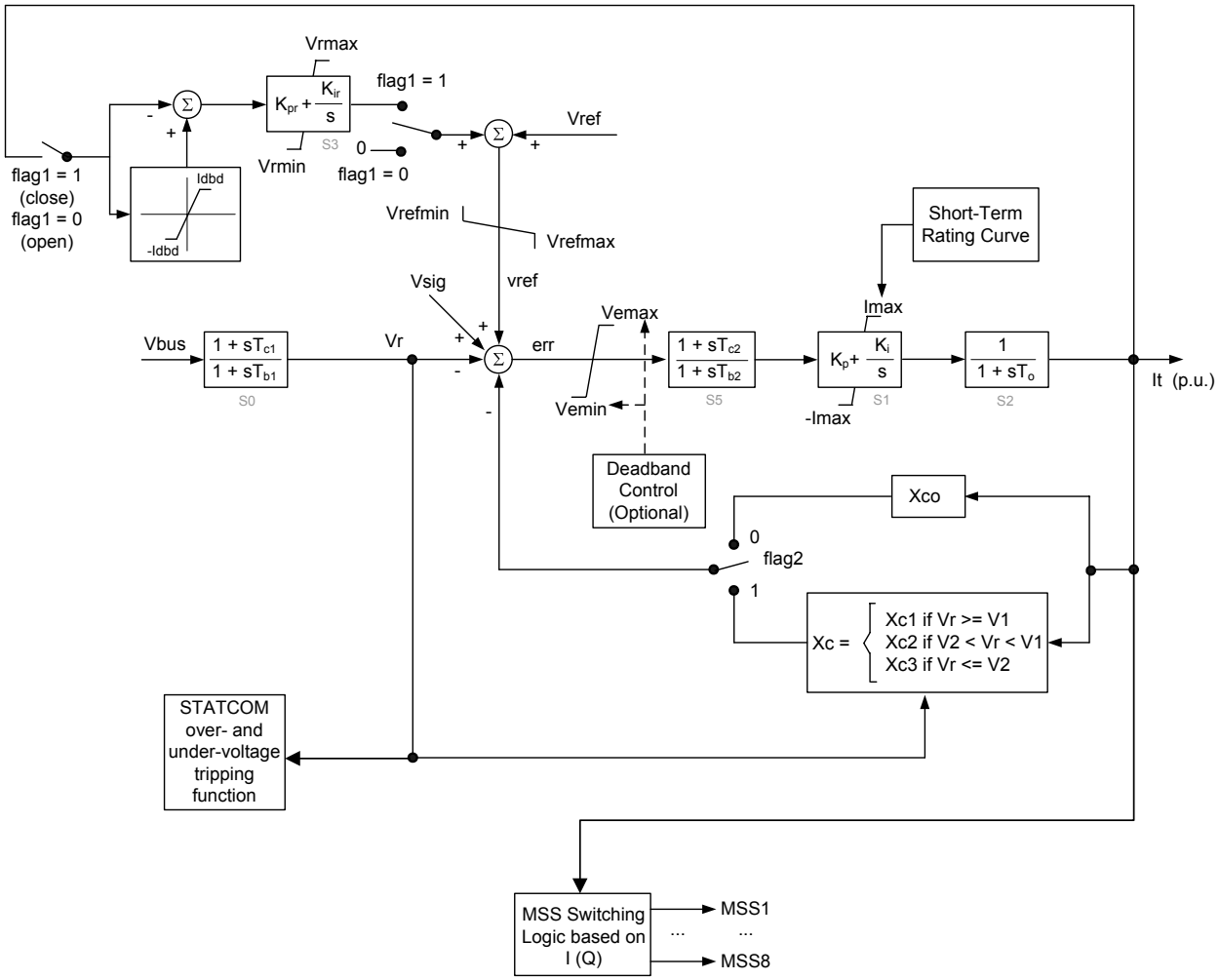

Figure 2-12: The generic SVSMO3 model of a VSC-based SVS.

The full parameter list for the model is provided in Appendix D. With the parameter list in mind, the key differences are described below:

1. VI Characteristic of the STATCOM: Figure 2-13 shows the voltage-current (VI) characteristic of the STATCOM for the SVSMO3 model. This is **not** an exact representation of the actual VI characteristic of any commercial STATCOM, but rather an emulation of the general behavior of this type of equipment for the purposes of power system planning studies. As shown in the figure, the STATCOM becomes a constant current device at its limits (+/- Imax1). For a short-time period (explained further below) this limit may go up to Ishrt times higher (red dashed line in the figure). If the voltage falls below UV1 the current limit is linearly reduced until the voltage reaches UV2. Once the voltage falls below UV2 the current limit becomes zero (i.e. the STATCOM is blocked). If the voltage exceeds Vtrip for more than Tdelay2 the model status is changed to zero and the unit trips. Between OV1 and OV2 the current limit changes linearly. If one wishes to emulate the effect of the unit step-up transformer (and series reactor) without explicitly modeling these, it can be done through the use

of OV1 and OV2, in the following way. Let us assume that at the terminals of the converter the controls do not allow the voltage to exceed 1.1 pu, i.e. the STATCOM blocks above this voltage. Furthermore, assume that the combined impedance of the unit transformer and any series reactor is 0.1 pu on the MVA based of the STATCOM. Let us further assume that the short-term current rating of the converter is 1.5 pu. Then at its capacitive limit for the voltage to be arrested to 1.1 pu at the STATCOM terminals, that means that the system voltage will be = 1.1 – 1.5 x 0.1 = 0.95 pu; thus OV1 = 0.95 pu. Similarly, at its inductive limit the system voltage would be = 1.1 + 1.5 x 0.1 = 1.25 pu; thus OV2 = 1.25 pu. In this way the SVSMO3 model can be used to model the device at the system voltage level and "implicitly" (rather than explicitly) account for the effect of the unit transformer.

If the user wants to model the unit transformer explicitly, then OV1 and OV2 are set to the same value to achieve a fixed current limit at the terminals of the voltage source converter.

2. Short-Term Rating: The short-term rating is a multiplier (Ishrt) on the continuous rating (Imax1) of the STATCOM. The allowable time for the short-term rating may be simulated as either a definite time delay (Tdelay1) or a thermal rating of the power-electronics represented by a I-squared time model (I2t, Reset and hyst). The logic of the I2t model is shown in Figure 2-14 (taken from [9]). This is a simplified representation of an actual physical process and sophisticated controls. By no means should it be assumed that this is a representation of the actual control logic for any such device. Only one of these should be used and they should not be used together. If the parameter I2t is zero then the definite time delay is used, otherwise the I2t limit is used. Use of the definite time delay is suitable for most planning studies.

3. Deadband: The deadband implementation in this model is slightly different from the other two models. In this case, if the voltage moves outside of the deadband (i.e. Vref – dbd < Vr < Vref + dbd) it must come back to within 1/Kdbd times this deadband (i.e. Vref – dbd/Kdbd < Vr < Vref + dbd/Kdbd) for more than Tdbd for the STATCOM to freeze again. The logic is shown in Figure 2-15.

4. MSS Switching: The logic for MSS switching is similar to SVSMO1 and SVSMO2. The differences are that the MSSs are switched based on reactive current (not susceptance), and that there is only one pair of switching points (Iupr/Ilwr) rather than two. This is more typical for STATCOMs as presently most STATCOM applications are smaller units and employ deadband for conserving dynamic range.

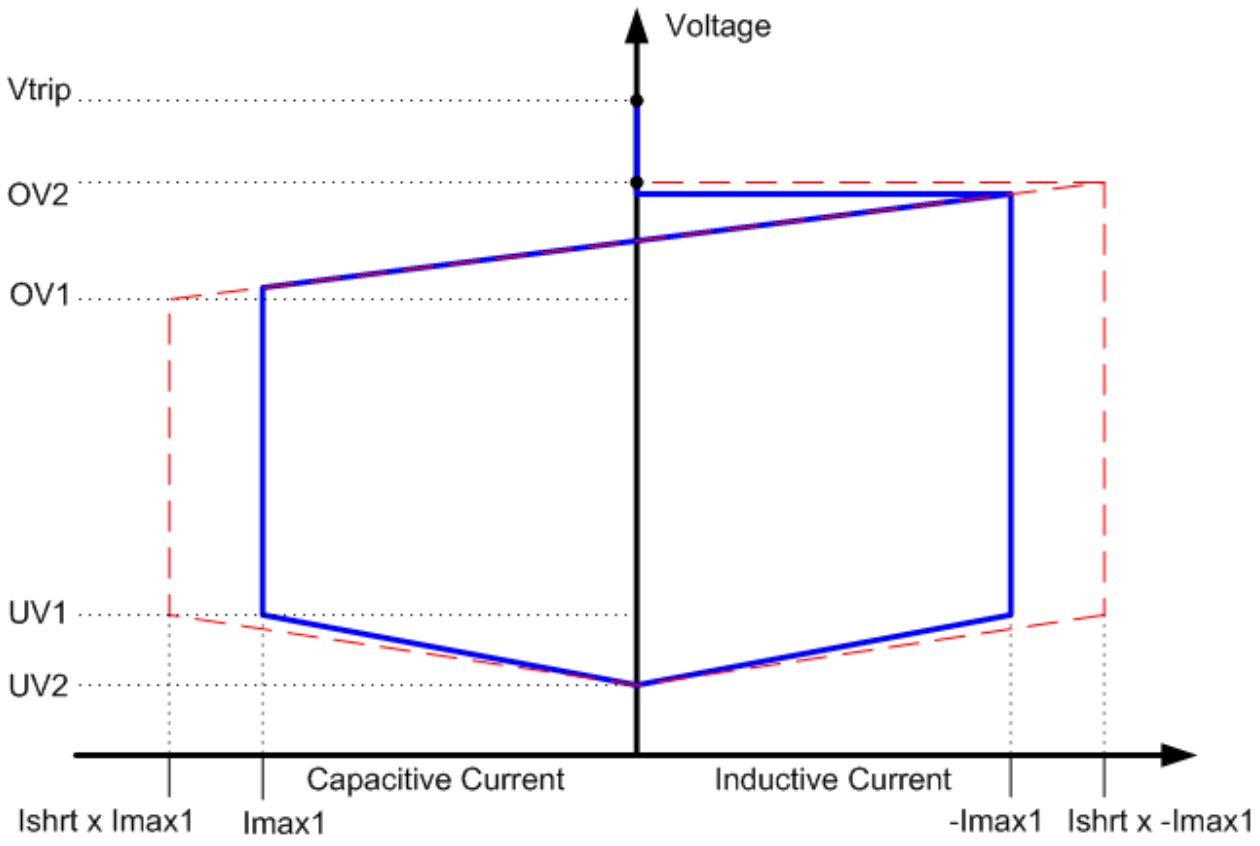

Figure 2-13: VI characteristic of the SVSMO3 model.

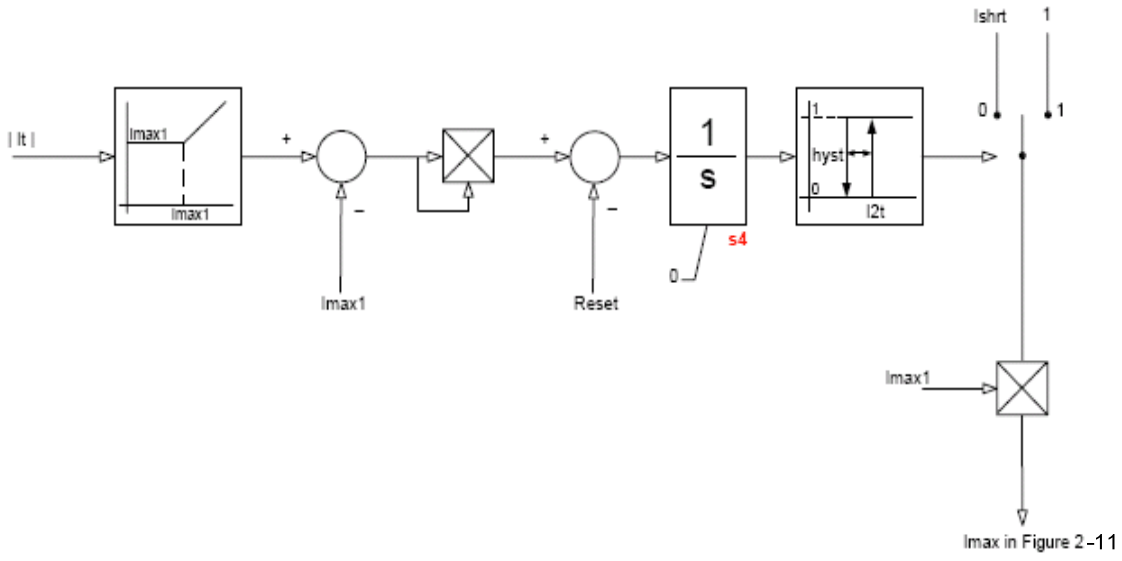

Figure 2-14: I2t short-term rating logic (figure reproduced from [9]).

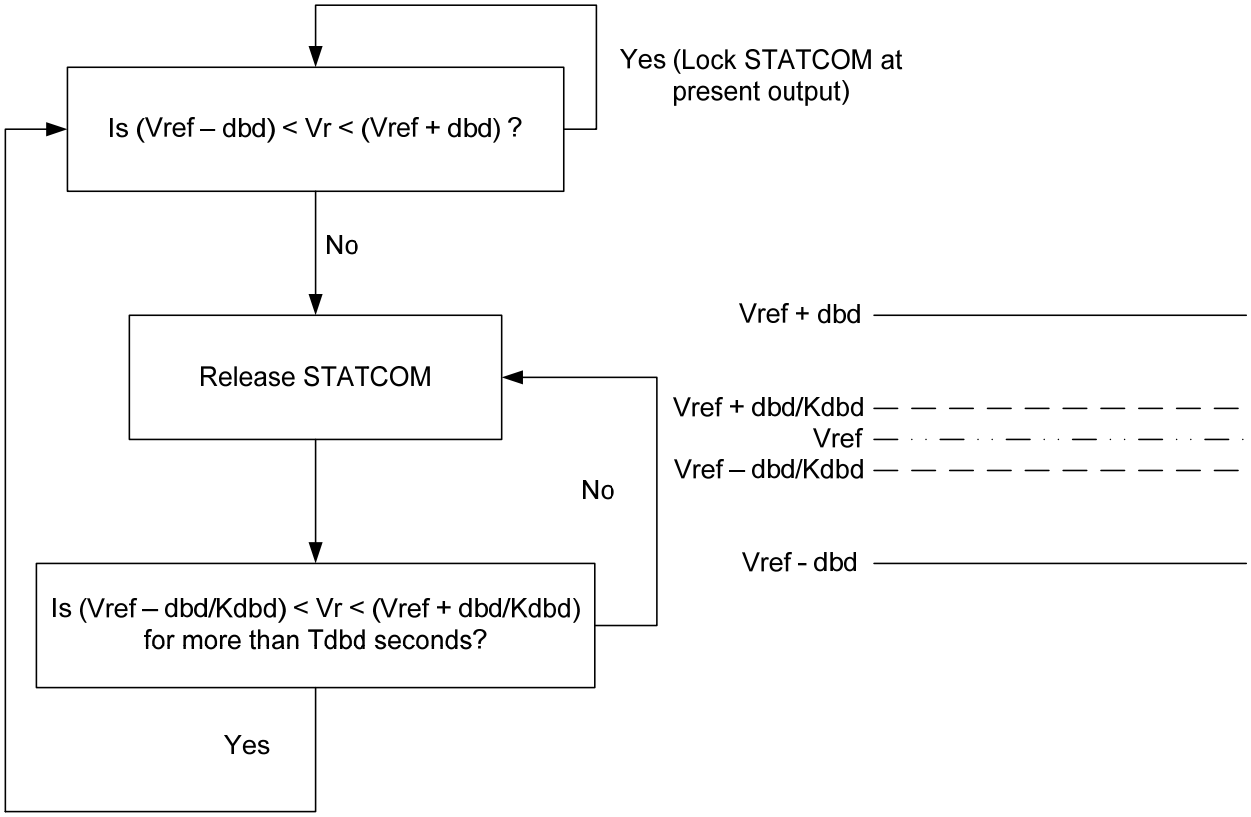

Figure 2-15: Deadband logic.

2.2 The Powerflow Model

Three new dynamic models have been developed these are,

- SVSMO1 – this is a generic SVS model incorporating an SVC and coordinated MSSs, where the SVC is assumed to consist of at least one TCR branch resulting in a smoothly controlled device coordinated with the discrete mechanically-switched MSSs.

- SVSMO2- this is a generic SVS model incorporating an SVC and coordinated MSSs, where the SVC is assumed to consist only of TSR and/or TSC branches resulting in a fast switched discrete device coordinated with the relatively slower discrete mechanically-switched MSSs.

- SVSMO3 – this is a generic SVS model incorporating a STATCOM and coordinated MSSs, resulting in a smoothly controlled device coordinated with the discrete mechanically-switched MSSs.

From a powerflow (steady-state) modeling perspective, a few aspects need to be implemented in any software platform to support these dynamic models. First, the SVS needs to be explicitly represented as a controllable shunt device in the powerflow model and not as a generator. Once this is done, the specific features of the controllable shunt device model are as follows:

- MSS Switching Logic: For each of the three SVS models, logic in the powerflow data structures allows the shunt SVS model to control fixed shunts in the shunt tables, thereby effecting coordinated control of MSSs during the power flow solution. The logic implemented is as follows:

  - Each fixed shunt has three attributes/parameters associated with MSS switching:

    i. switching status = 1 if it is available to be switched by the SVS, or 0 if not.

    ii. the bus number of the controlling SVS

    iii. the id of the controlling SVS

  - Each SVS model has three attributes/parameters associated with MSS switching:

    i. Bminsh – this is the minimum susceptance (for thyristor based SVCs) below which the SVC will either switch off a shunt capacitor or switch in a shunt reactor, whichever is available in the shunt table (in the order they appear) for switching by the SVC.

ii. Bmaxsh – this is the maximum susceptance (for thyristor based SVCs) above which the SVC will either switch in a shunt capacitor or switch out a shunt reactor, whichever is available in the shunt table (in the order they appear) for switching by the SVC.

The goal of this switching logic is to attempt, to the extent possible, to maintain the dynamic range of the SVC by switching the coordinated MSSs controlled by the SVC to keep the SVC output between Bminsh and Bmaxsh. Reference [1] provides an actual practical example of this control logic. Figure 2-16 gives a generic illustration of how this logic functions and is implemented in powerflow.

For the VSC based SVS, the logic is the same, however, we have switching on current rather than susceptance.

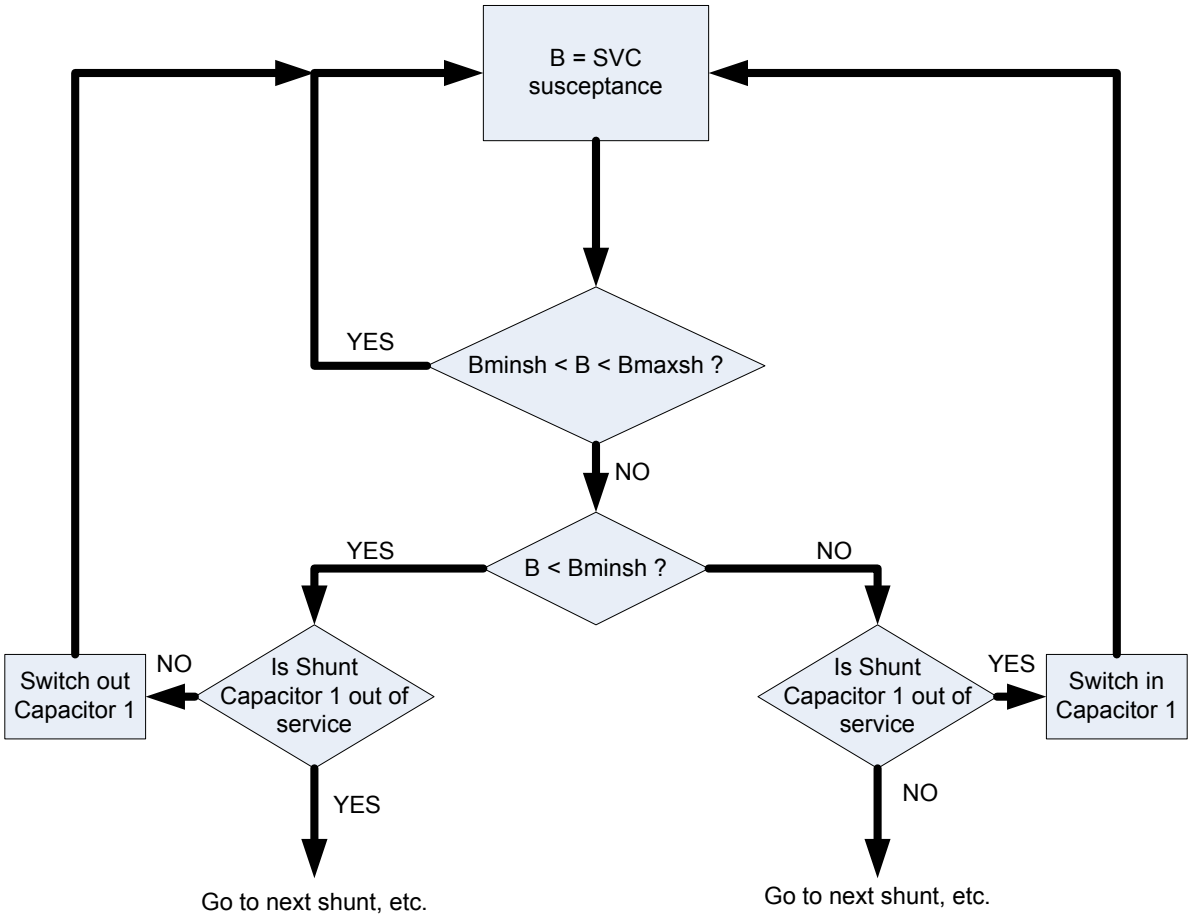

Figure 2-16: Flow chart for the MSS switching logic.

o Slope: For each of the three SVS models, logic is implemented to represent a linear slope, using one parameter Xc (ratio of voltage change to current change over the defined control range of the device). For example, if a 3% voltage change is allowed across the entire control range of an SVC, and the

SVC is rated +200/-100 Mvar and we assume a system MVA base of 100 MVA, then the slope is Xc = 0.03/3 = 0.01 pu on 100 MVA base[8]. The inherent assumption is that the SVS has an integral (or PI) control. Therefore, in steady-state (as along as it has not run out of capacitive/inductive range) the SVS will act until Vcomp is equal to Vsched (see Figure 2-1). Vcomp = Vbus + Vbus x Bsvc x Xc, where Vbus is the actual bus voltage. The SVC output (Bsvc) is limited to stay within Bmax/Bmin. When the case solves the actual bus voltage will be Vbus = Vsched – Vbus x Bsvc x Xc, if the slow-suceptance regulator is inactive.

o Slow susceptance regulator: The slow-susceptance regulator of an SVS can be modeled in the powerflow as described below. The algorithm is based on that developed in [2]. The following six attributes/parameters are associated with the SVS powerflow model:

- one parameter to turn this function on (1) or off (0),
- two parameters (Bminsb and Bmaxsb) to define the range of B within which the SVC output is to be kept in steady-state. This is similar to the MSS switching logic.
- two parameters (Vrefmax and Vrefmin) to define the range of allowable voltage reference change by the SVC to keep the B output within Bminsb/Bmaxsb (see explanation of slow-susceptance regulator below or [2]).
- a parameter (dvdb) for the user to specify the voltage gradient as a function of Vars at the SVS bus, that is, $\partial V/\partial Q$. This can be estimated from the short-circuit impedance at the bus. Namely, if the positive sequence, 3-phase short circuit impedance at the SVS transmission bus is Z pu, then by Ohm's Law one can see that $\partial V/\partial Q$ is approximately equal to Z pu. The reason for this parameter is explained below in the algorithm –see also [2].

The proposed algorithm is as follows:

vrefmax (maximum allowable voltage schedule at the bus)

vrefmin (minimum allowable voltage schedule at the bus)

[8] Note: The IEEE Guide 1031 defines the per unit base upon the entire range of the SVC and this is widely used by the manufacturers, but because the models commonly use system MVA base (e.g. typically 100-MVA) the slope needs to be placed on this base.

First solve the powerflow for one iteration to hold the current bus scheduled voltage (including slope)

then set vref = vsched

If (the slow susceptance regulator is in-service)

If Bmaxsb < Bsvc < Bminsb

Take no action

else

- Lower/raise vref (the controlled bus voltage reference) until SVC output is between Bmaxsb/Bminsb. To lower/raise the vref the following algorithm is used:

- From the input by the user we have dvdb = $\partial V/\partial Q$. Now change vref as follows:

If (Bsvc > Bmaxsb)

vref = vref + (Bmaxsb - Bsvc)×dvdb

elseif (Bsvc < Bminsb)

vref = vref + (Bminsb - Bsvc)×dvdb

end

- vref must ALWAYS be between vrefmax & vrefmin, i.e., if it hits one of these limits then stop.

end

end

Iterate until convergence.

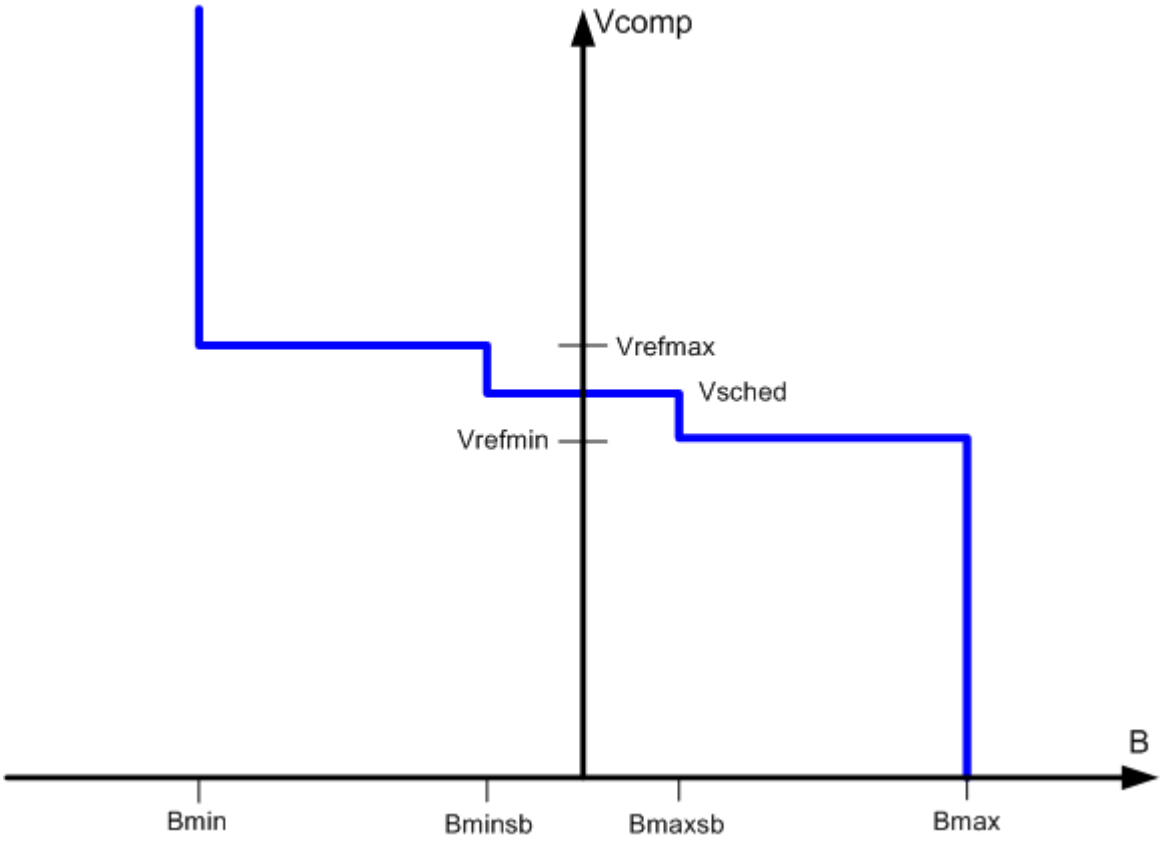

Figure 2-17: Steady-state powerflow boundary conditions of the SVC slow-susceptance solution.

An alternate means of expressing the powerflow solution algorithm described above is shown by Figure 2-17. This figure shows the boundary condition at the SVC bus. The horizontal line at Vcomp=Vsched represents the condition in which the SVC is able to hold the scheduled voltage without exceeding the susceptance bounds Bmaxsb or Bminsb (i.e., the algorithm requires only one step to complete). The vertical line at B=Bminsb indicates the condition where the slow-susceptance regulator determines that the magnitude of the susceptance is minimal and hence does not perform any further action; similarly, the slow susceptance regulator will not perform any further action to reduce B on the vertical line at B=Bmaxsb. The horizontal line at Vcomp=vrefmax (or Vcomp=vrefmin) represents the condition in which the slow susceptance regulator takes no further action because voltage is not allowed to exceed vrefmax (or fall below vrefmin). Finally, the absolute susceptance limits of the SVC (Bmin and Bmax) are represented by vertical lines on the V/B plane.

It should be emphasized that the above powerflow algorithm is a simplified representation of the slow-susceptance regulator for steady-state analysis. Thus, the final steady-state equilibrium condition of an SVC at the end of a dynamics simulation will not necessarily be the same as that obtained by the powerflow

solution. One reason for this is the action of the MSS switching, which may occur due to, for example, a nearby fault. This is explained below.

It is pertinent to explain the goal of the coordinated MSS switching and slow-susceptance regulator as they work in complement to each other. The objective of both functions, is to reduce the output of the SVC to keep the fast smoothly control reactive output of the SVC in reserve. Consider Figure 2-18. On the left hand side of the figure is shown the dynamic model of the slow-susceptance regulator. This regulator acts on comparing the actual susceptance (output) of the SVC to the given reference (single value) or more typically/generally a range of values (Bminsb to Bmaxsb). If the susceptance (B) lies in this range (or at the reference) nothing is done. If B is outside the range, then the voltage schedule (reference) of the SVC is slowly (over typically many tens of seconds to minutes) biased by a proportional-integral regulator[9] until the SVC B enters within the desired range. Now consider the right hand side of the figure. Consider the SVC at a steady-state operating condition A; at this point the bus voltage is at the scheduled voltage and within both the B-limits (Bminsb < B < Bmaxsb). Now let us assume a fault occurs somewhere out on the system and a major line is tripped. This will push the SVC output to point B to try to maintain the bus voltage. Subsequently, if the SVC is controlling local shunt capacitors (MSCs) it will quickly switch in a shunt to reduce its output and take it to point C – note: the MSS switching logic typically has two levels one for fast switching presented in this example and one for slow switching for steady-state regulation (discussed above), all these functions need to be coordinate (e.g. see [1]). Now at point C, however, we are still outside of the Bmaxsb/Bminsb band. Thus, the slow susceptance regulator now acts to slowly bring the SVC output back inside the "green box" by allowing the SVC reference voltage to be slightly biased by the slow susceptance regulator action and thus lowering the bus voltage a small amount (typically 1% or less). The voltage is never allowed to go outside of Vrefmax/Vrefmin, which are operator set limits (e.g., 1.02 to 0.98 pu). All this achieves voltage stability, regulation and helps to maintain reactive power reserves.

In time-domain simulations all of the above actions are simulated. However, in powerflow steady-state analysis we cannot know what the initiating event is (e.g. fault, tripping of a line due to miss-operation, etc.), therefore, the behavior of the MSS switching and slow susceptance regulator are emulated to the extent possible by the algorithms presented above.

[9] Most commonly the regulator is an integral control with no proportional gain; a proportional-integral regulator has been modeled for generality.

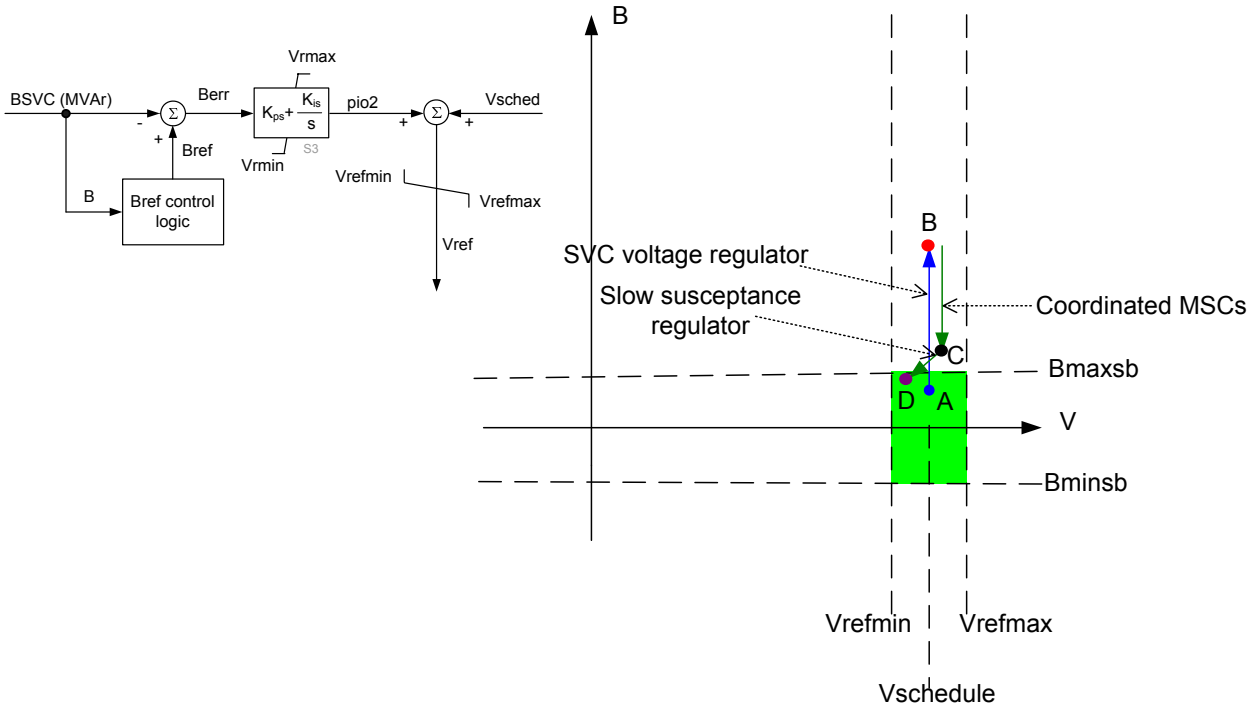

Figure 2-18: Functioning of the slow-susceptance regulator.

An important note for the user is to understand that the actual bus voltage, after convergence of the powerflow solution, may not be exactly equal to the scheduled voltage (Vsched). If a proper powerflow solution is reached, the reason for this difference is driven by two actions of the SVS controls: (i) a non-zero slope (Xs), and (ii) the action of the slow-susceptance regulator, which deliberately acts to bias the scheduled voltage to bring the steady-state output of the SVC to within the desired steady-state reactive power output bandwidth (Bminsb and Bmaxsb) – see Figure 2-1.

The distinction between the three models in powerflow is as follows:

1. SVSMO1 – should have all the features above and the SVC component is continuously controlled.
2. SVSMO2 – the SVC in this case is a discrete device made up of several branches. Thus, the possible B output of the SVC is comprised of all the unique combinations of the multiple-braches. This is explained in more detail in section 2.3.2.
3. SVSMO3 – the STATCOM part of this model becomes a constant current source (instead of a passive element) at its limit.

Much of the write-up for this section has been taken from [13].

3. MODEL VALIDATION

The model presented here is based on the one reported in [1], [2] and [8]. The main difference is in the addition of some of the more generic features:

1. deadband control
2. non-linear slope/droop
3. the extra lead/lag block

Apart from these features, the core of the model is essentially identical to those in [1], [2], and [8].

In [1], the model was validated against a detailed vendor PSCAD™ model of the actual SVC controls. In [8], the model was verified against an actual DFR recording of the SVC response following a major system disturbance. In this case, many of the salient features of the model were verified; the under-voltage strategy, the slope, the main voltage regulation loop, etc.

In summary, this model is quite suitable for use in power system simulation and can reliably capture all the relevant dynamics of a modern SVC system.

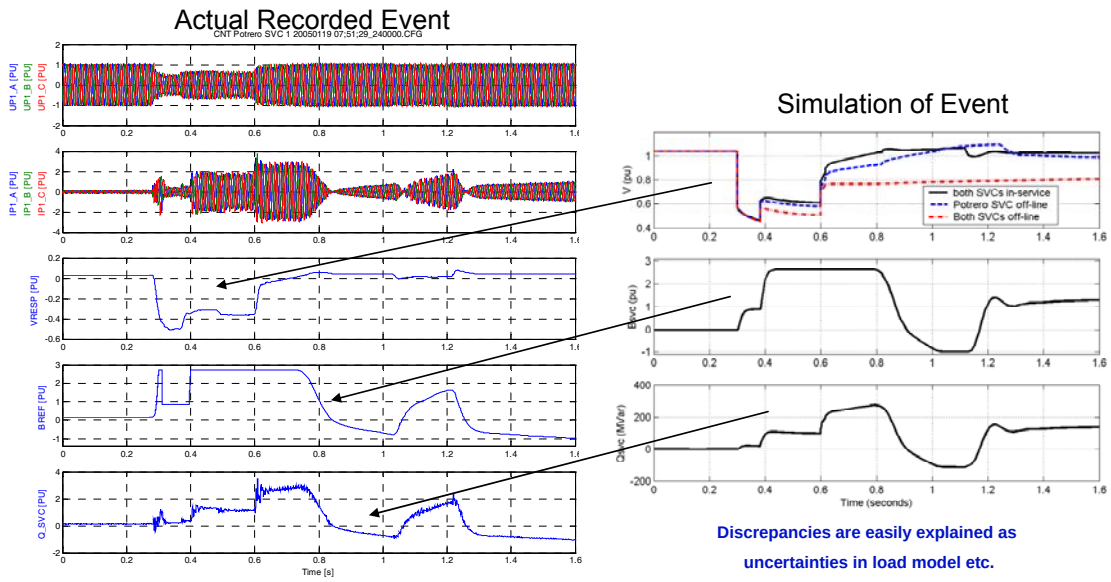

Figure 3-1: Example model validation (from [8], © IEEE 2006).

The data for the above event — the digital fault recorder (DFR) recording — was provided by ABB to EPRI. Using a similar technique to that described in [12], the DFR data was used by to validate the SVS model shown in Figure 2-1. By feeding the measured transmission system voltage into the model and fitting the susceptance and Q (reactive power) response – see Figure 3-2– the model was

validated. This illustrates an example of model validation for a FACTS device. The recorded response of the SVC was captured by the digital fault recorder (DFR) that is built-in the SVC control system.

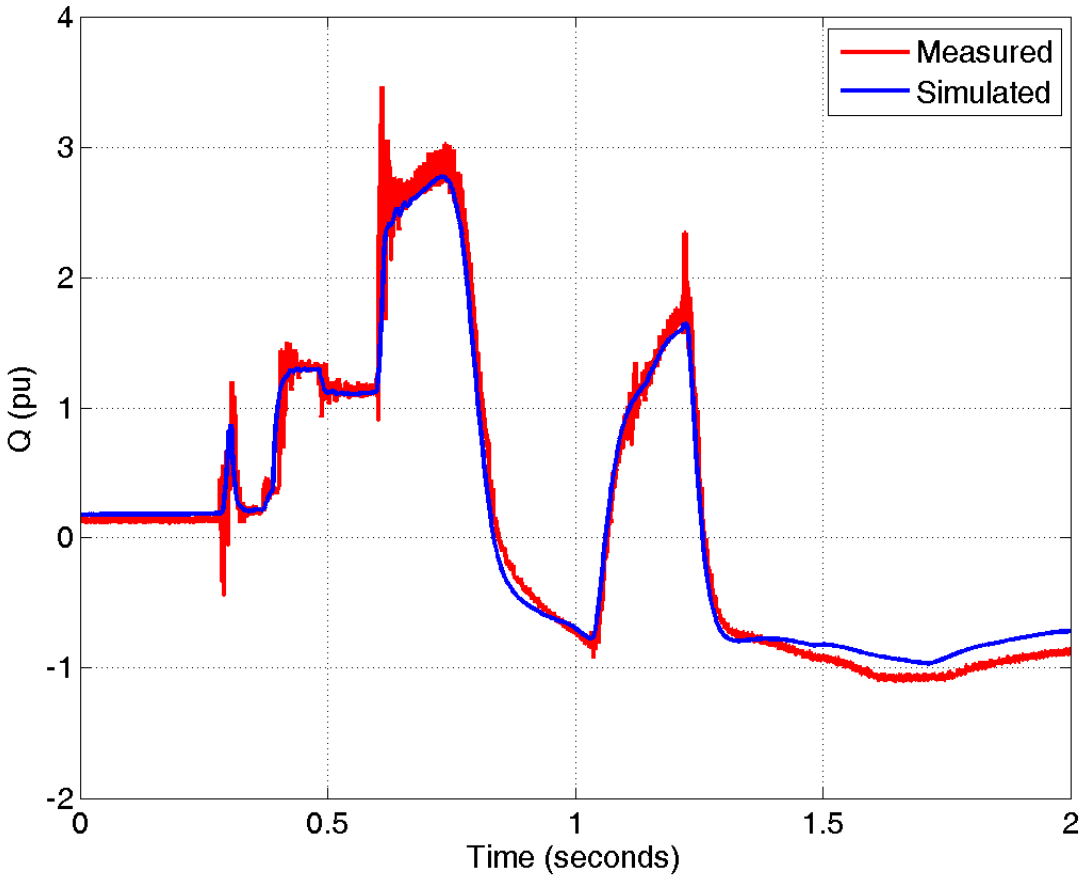

Figure 3-2: Measured and simulated reactive power output response of a transmission SVC installation. Response is to a delayed clearing of a transmission fault (see [8] for a description of the event).

Similarly, ABB provided data for another system event for a different SVC installation. This too was easily validated, see Figure 3-3.

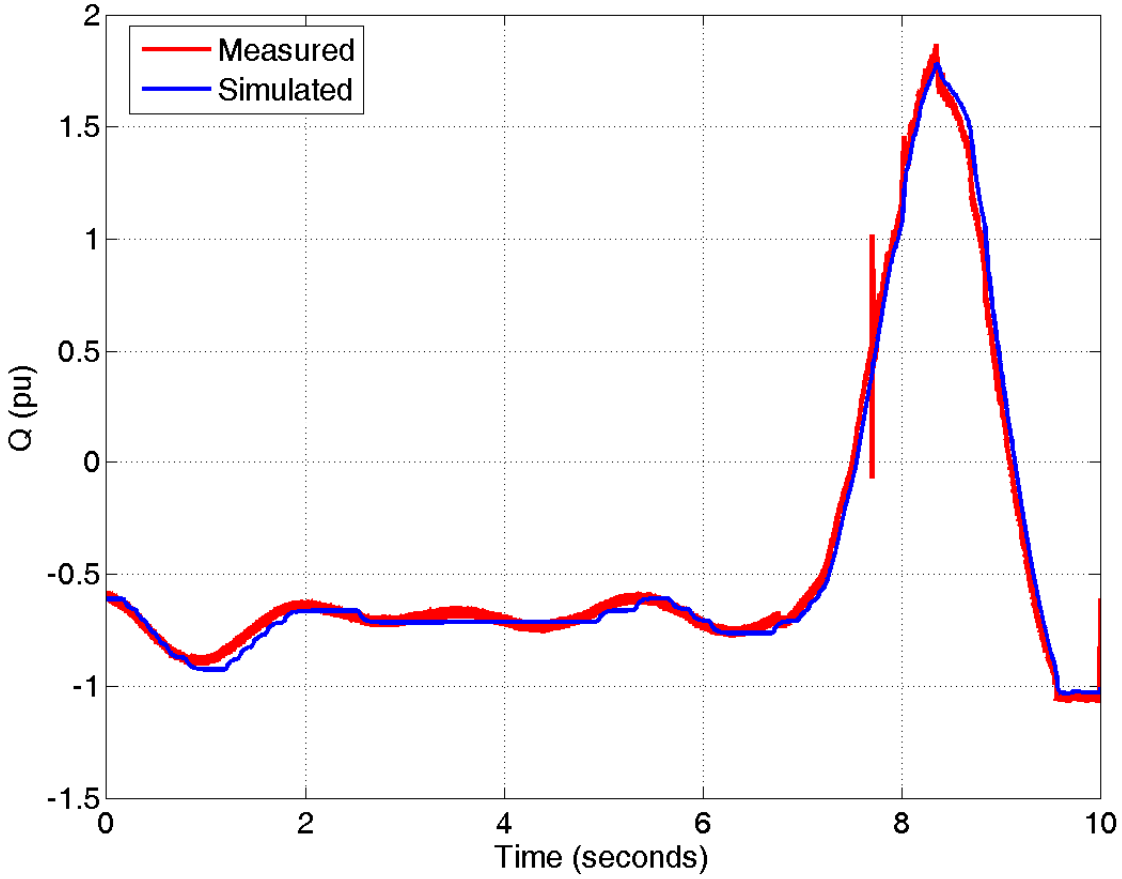

Figure 3-3: Measured and simulated reactive power output response of a transmission SVC installation. Response is to a WECC-wide event.

Model validation similar to that shown above in Figure 3-2 and Figure 3-3 has also been demonstrated by EPRI, for an unbalanced fault also (see Figure 3-4).

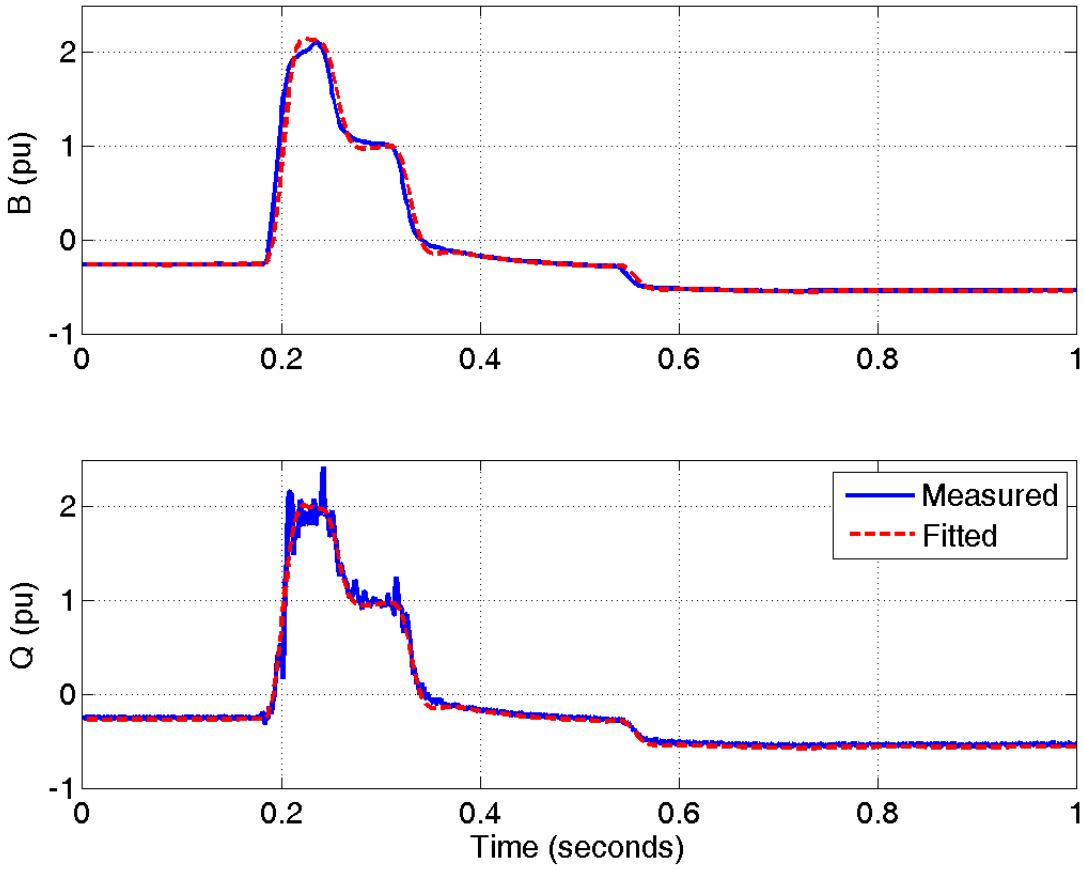

Figure 3-4: Measured and simulated reactive power output and susceptance response of a transmission SVC installation. Response is to an unbalanced fault.

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18. P. Pourbeik and M. J. Gibbard, “Damping and Synchronizing Torques Induced on Generators by FACTS Stabilizers in Multimachine Power Systems”, IEEE Transactions on Power Systems, November 1996, pages 1920-1925.
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A. SVC DYNAMIC MODEL TESTING FOR THE TCR-BASED SVS MODEL

1.0 Objective

The objective of this task is to test and validate the features and performance of a generic SVC dynamic model.

This test plan should be considered a supplement to the "Generic SVC Model for WECC" document prepared by the WECC SVC Modeling Task Force of the Modeling and Validation Working Group.

2.0 Description/Specification Benchmark test system

The test system is depicted in Figure A-1 below.

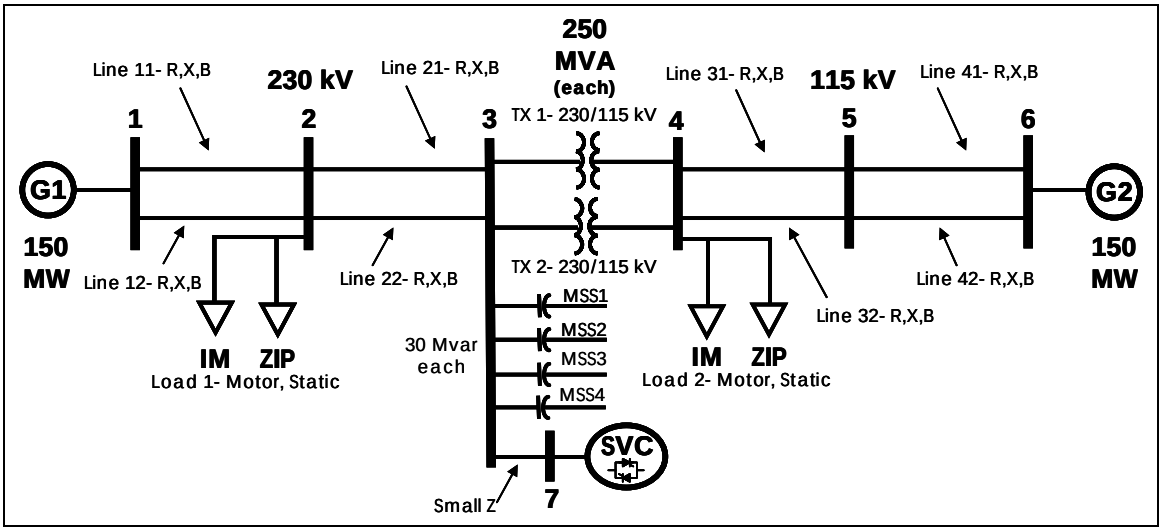


Figure A-1. Simplified One-Line for Test System Model

The following are characteristics of the test system model:

1) Bus 6 is the swing bus at 1.0 pu.
2) Generator 1 and 2 each has an exciter model and generator dynamic model.

   exciter = exst4b, generator = genrou

   G1 = G2 = Pmax, Qmax/Qmin = 150 MW, +/- 45 Mvar
3) Each line segment is modeled as a 25-mile overhead transmission line.

   Line 11 Impedance = 12 = 21 = 22 => R,X,B = 0.003 pu, 0.0332 pu, 0.051 pu (Zbase=529Ω)

   Line 31 Impedance = 32 = 41 = 42 => R,X,B = 0.023pu, 0.134 pu, 0.0152 pu (Zbase=132Ω)

4) The load composition at bus 2 and 4 is 40% induction motor and 60% static.

   Load 1 = Pload, Qload = 100 MW, 30 Mvar

   Load 2 = Pload, Qload = 115 MW, 30 Mvar

5) The transformer impedance(s) at bus 3 is 0.0564 pu on 252 MVA.

6) The SVC rating is -50/+200 Mvar connected at 230 kV (bus 7). The SVC is modeled as a generator in the powerflow with Qmin and Qmax set at SVC rating (-50/+200 Mvar). The scheduled voltage to achieve near zero output is 1.006 pu.

Figure 2-1 shows the general block diagram of the generic SVC model under test.

The following features of the generic SVC dynamic model are to be tested:

1) PI voltage regulation loop
2) Lead/lag voltage measurement (Tc1/Tb1)
3) Lead/lag for transient gain reduction (Tc2/Tb2)
4) Slow susceptance regulator
5) Over/undervoltage protection
6) Deadband control
7) Non-linear slope (droop)
8) MSS logic
9) Lag block (T2)

3.0 Case List

Table A-1 presents the overall case list for testing the generic SVC dynamic model being considered by the WECC SVC Modeling Task Force.

Table A-1 – Case List for Testing the Generic SVC Model

Case Number	Event Description	Fault Location	Fault Impedance	Fault Clearing Time	Branch Cleared	Comment
1	Fault	Bus 2	0	6 cycles	Line 22	
1b	Fault	Bus 2	0.01+j0 pu	9 seconds	n/a	Test UV Trip
1c	Fault	Bus 2	0.1+j0.1 pu	9 seconds	n/a	Test UV Trip
2	Fault	Bus 3	0	6 cycles	TX2	
3	Fault	Bus 5	0	6 cycles	Line 42	
3a	Fault	Bus 5	0	6 cycles	Line 42	Illustrate slow voltage recovery
4	Fault	Bus 3	0	6 cycles	Line 21 & Line 11	Unstable
5	Fault	Bus 4	0	6 cycles	Line 31 & Line 41	
6	Step change	n/a	n/a	n/a	n/a	
6a-6e	Step change	n/a	n/a	n/a	n/a	Slope variation
7	Step change	n/a	n/a	n/a	n/a	Variation of Kpv/Kpi
7a	Step change	n/a	n/a	n/a	n/a	Variation of Kpv/Kpi
8	Step change	n/a	n/a	n/a	n/a	Variation of Tc1/Tb1
8a	Step change	n/a	n/a	n/a	n/a	Variation of Tc1/Tb1
9	Step change	n/a	n/a	n/a	n/a	Variation of Tc2/Tb2
9a	Step change	n/a	n/a	n/a	n/a	Variation of Tc2/Tb2
10	Step change	n/a	n/a	n/a	n/a	Test Slow Susceptance Control
11	Inc Bus Voltage	n/a	n/a	n/a	n/a	Variation of overvoltage setting
12	Vary Bus Voltage	n/a	n/a	n/a	n/a	Test Deadband control
13	Vary Bus Voltage	n/a	n/a	n/a	n/a	Apply non-linear droop
14	Vary Bus Voltage	n/a	n/a	n/a	n/a	Switch MSSs
15	Step change	n/a	n/a	n/a	n/a	Variation of lag T2
16	Step change	Bus 2	0	6 cycles	Line 22	Apply POD control

POD to be tested after SVC model is incorporated in software library model

NOTE: Refer to Table A-2 for a list of input model parameters and their settings for each case in Table A-1.

For all simulations, apply the following assumptions:

1) The fault is bolted and symmetrical (zero impedance, three-phase).
2) The fault occurs one second after the start of the simulation.
3) Run each simulation for at least 10 seconds.
4) At a minimum, simulation plots will include SVC susceptance and regulated bus voltage.
5) Model input parameters for each case are shown in Table A-2.

4.0 Test schedule

Initial testing: June 2008 (discussed at Edmonton, Alberta meeting)

Update report (r2): Sept 2008 (reviewed at Albuquerque, NM meeting)

Update report (r3): Nov 2008 (test new model code to switch shunt reactors)

Update report (r4): Jan 2009 (final report for review)

5.0 Simulation Results

Case 1 – Fault Bus 2 and Clear Line 22

Case 1 demonstrates the generic SVC model's response to a fault near Bus 2 at 1 second in the simulation, with 6-cycle clearing of Line 22. Regulated bus voltage and SVC susceptance are shown in Figure A-2, with generator power swings shown in Figure A-3.

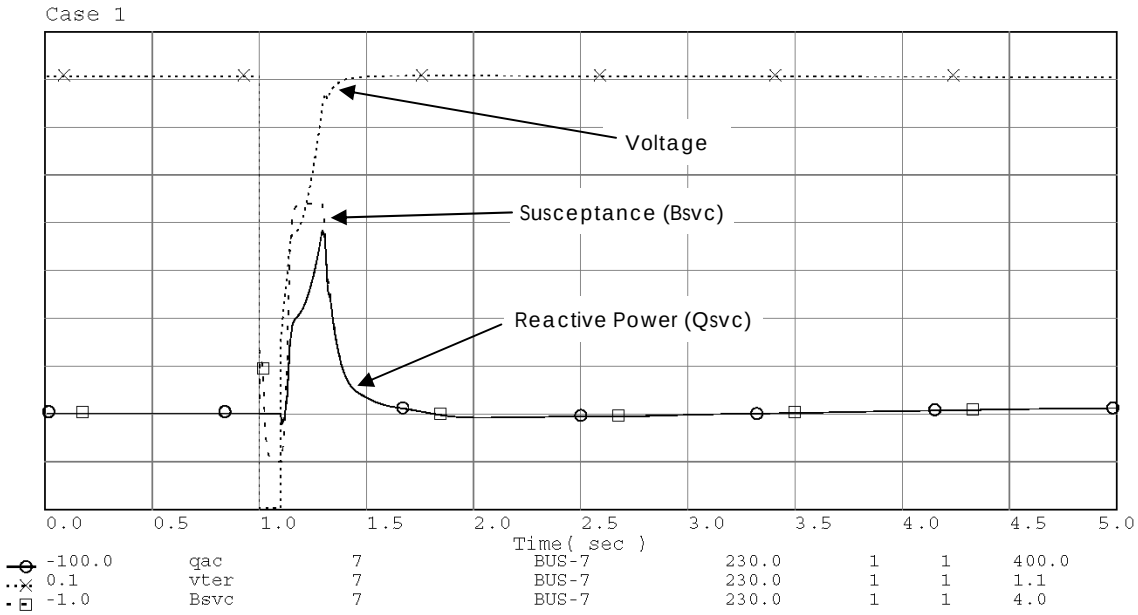


Figure A-2. Case 1 simulation result; voltage, susceptance, and reactive power.

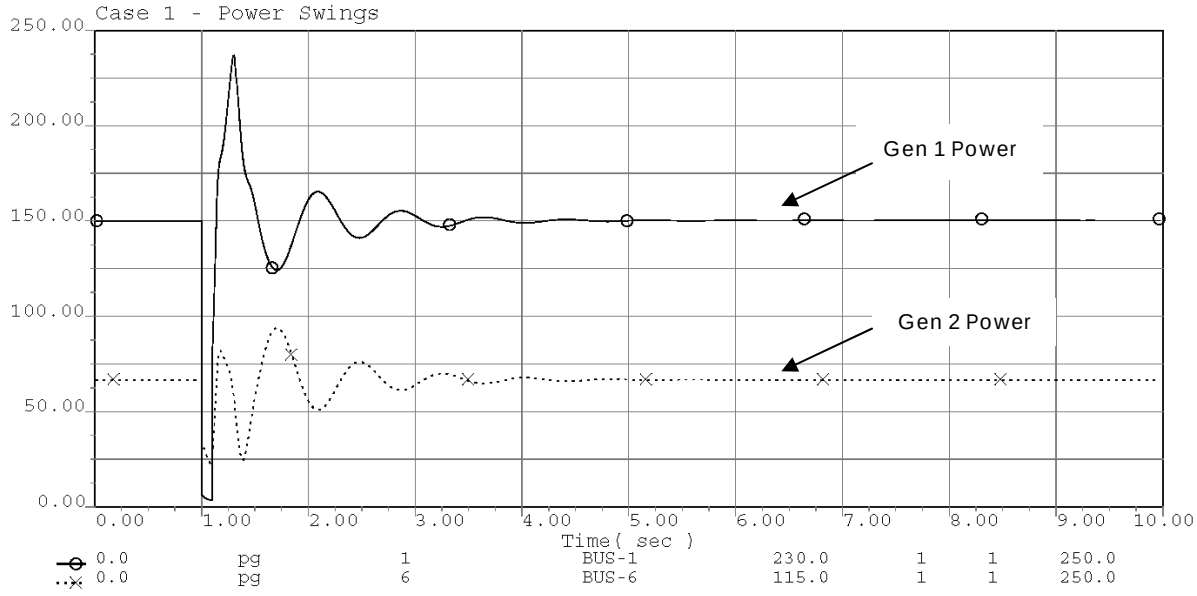


Figure A-3. Case 1 simulation result; power swings

Case 1b – Fault Bus 2 and Test UV2 Trip

Case 1b demonstrates the generic SVC model's response to a sustained fault near Bus 2 at 1 second in the simulation. The voltage fell below the UV2 threshold and then the UV2 timer elapsed after 7 seconds with voltage depressed. The SVC was then tripped off-line. Regulated bus voltage and SVC susceptance are shown in Figure A-4.

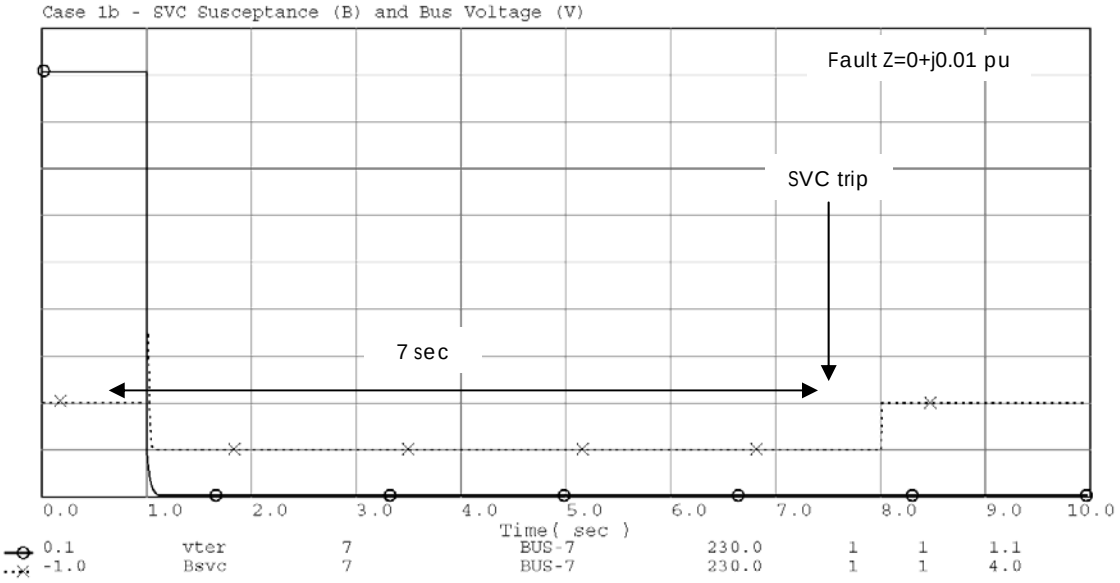


Figure A-4. Case 1b simulation result; undervoltage trip UV2

Case 1c – Fault Bus 2 and Test UV1 Trip

Case 1c demonstrates the generic SVC model's response to a sustained fault near Bus 2 at 1 second in the simulation. The voltage fell below the UV1 allowing the SVC output to be set to UVSBmax. The voltage continued down below UV2 and the SVC tripped off. Regulated bus voltage and SVC susceptance are shown in Figure A-5.

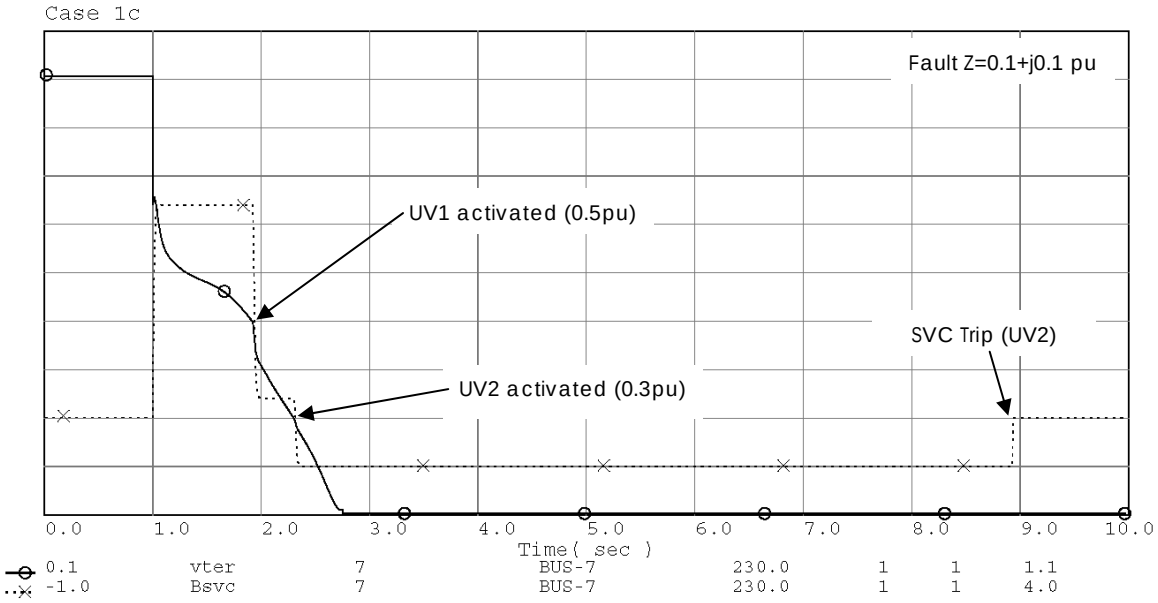


Figure A-5. Case 1c simulation result; undervoltage trip UV1 and UV2

Case 2 – Fault Bus 3 and Clear TX2

Case 2 demonstrates the generic SVC model's response to a fault near Bus 3 at 1 second in the simulation, with 6-cycle clearing of Transformer 2. Regulated bus voltage and SVC susceptance are shown in Figure A-6, with generator power swings shown in Figure A-7.

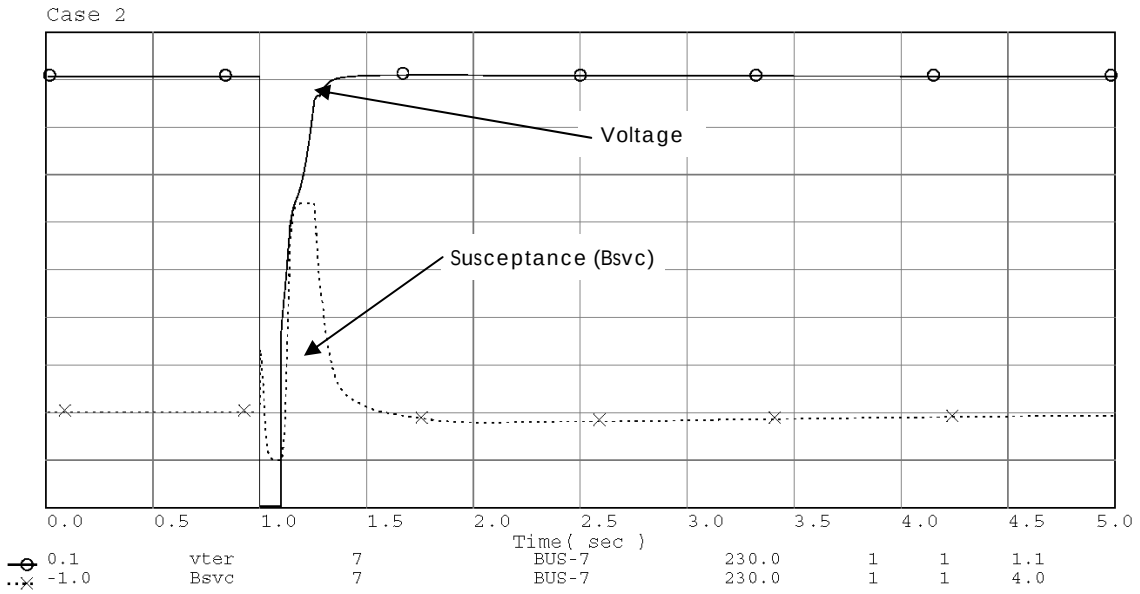


Figure A-6. Case 2 simulation result; voltage and susceptance.

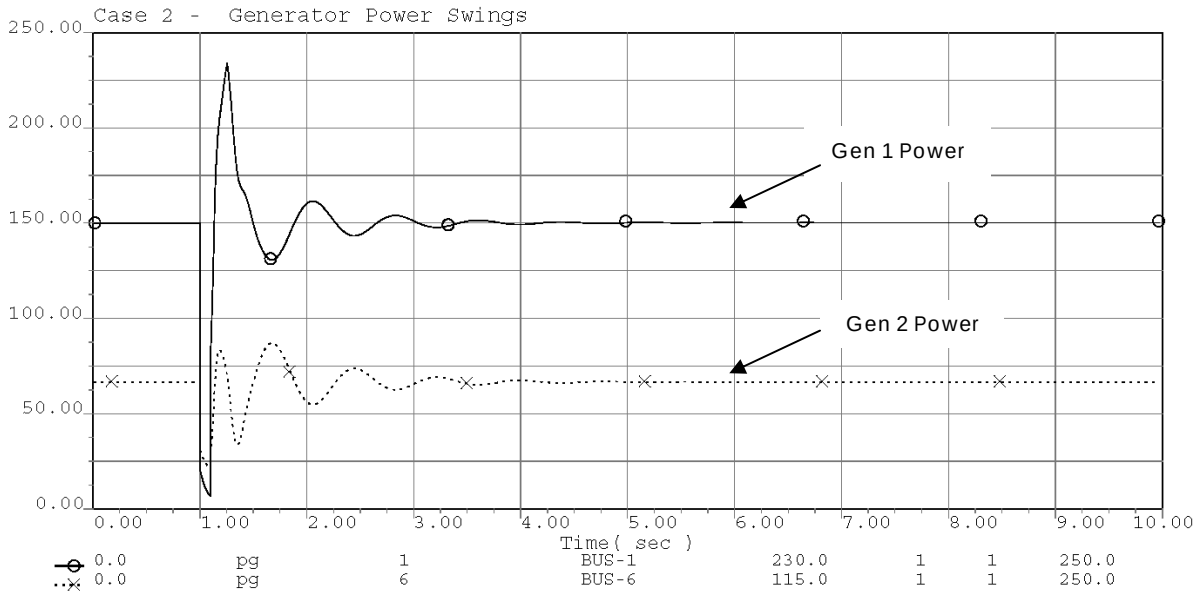


Figure A-7. Case 2 simulation result; power swings

Case 3 – Fault Bus 5 and Clear Line 42

Case 3 demonstrates the generic SVC model's response to a fault near Bus 5 at 1 second in the simulation, with 6-cycle clearing of Line 42. Regulated bus voltage and SVC susceptance are shown in Figure A-8, with generator power swings shown in Figure A-9.

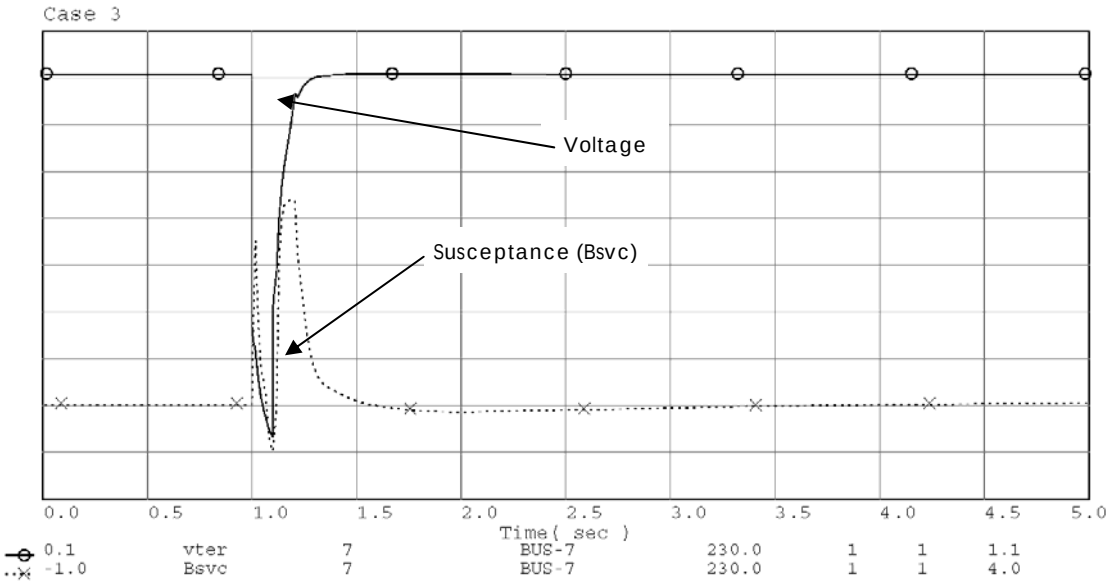


Figure A-8. Case 3 simulation result; voltage and susceptance.

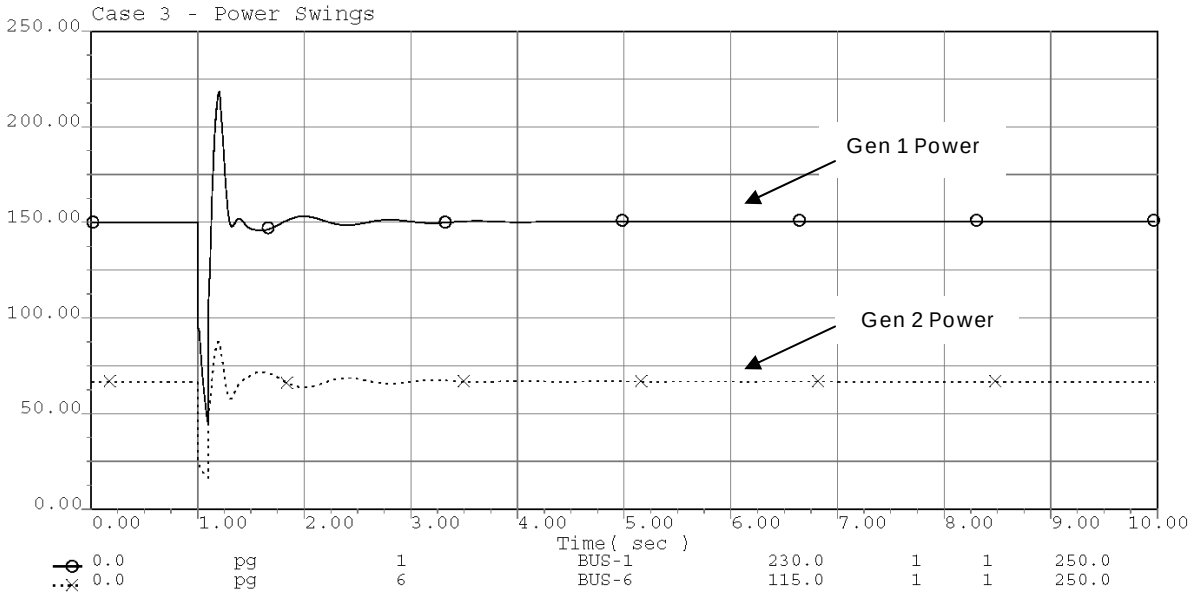


Figure A-9. Case 3 simulation result; power swings.

Case 3a – Fault Bus 5 and Clear Line 42 with Delayed Voltage Recovery

Case 3a demonstrates the generic SVC model's response to a fault near Bus 5 at 1 second in the simulation, with 6-cycle clearing of Line 42 generator excitation systems turned off and motor load increased from 40% to 99%. Regulated bus voltage and SVC susceptance are shown in Figure A-10.

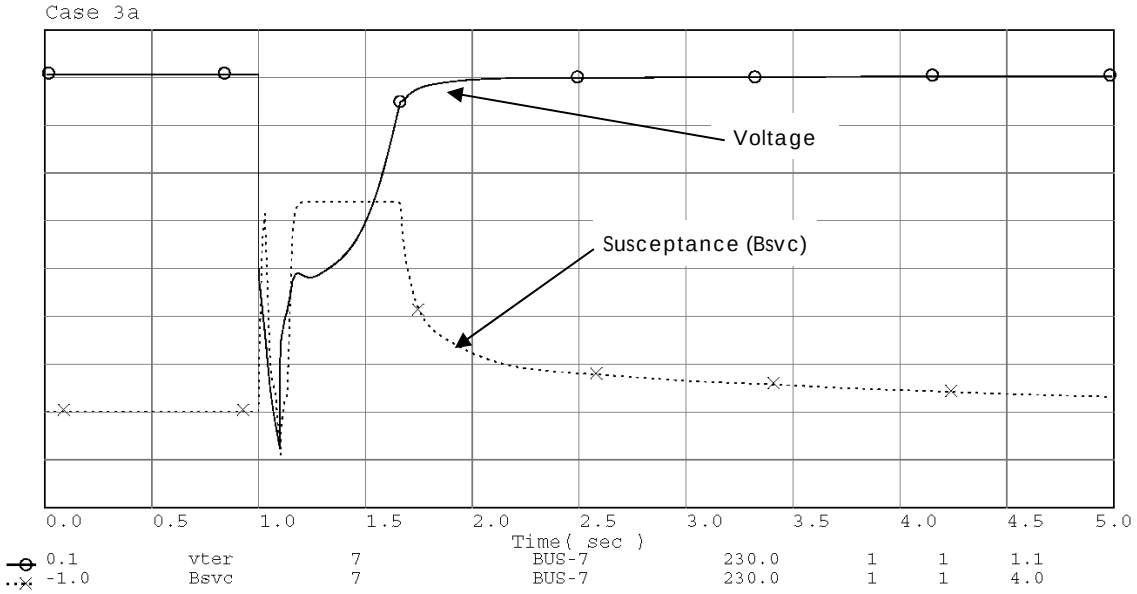


Figure A-10. Case 3 simulation result; voltage and susceptance.

Case 4 – Fault Bus 3 and Clear Line 21 and Line 11

Case 4 demonstrates the generic SVC model's response to a fault near Bus 3 at 1 second in the simulation, with 6-cycle clearing of Line 21 and Line 11. Regulated bus voltage and SVC susceptance are shown in Figure A-11.

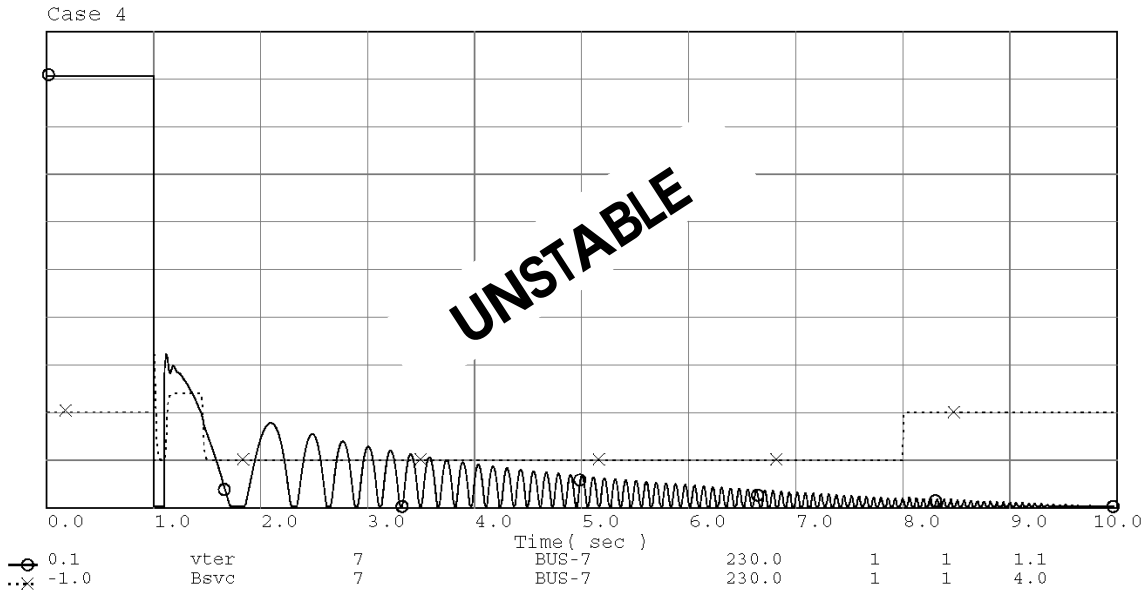


Figure A-11. Case 4 simulation result.

Case 5 – Fault Bus 4 and Clear Line 31 and Line 41

Case 5 demonstrates the generic SVC model's response to a fault at 1 second in the simulation near Bus 4 at 1 second in the simulation, with 6-cycle clearing of Line 31 and Line 41. Regulated bus voltage and SVC susceptance are shown in Figure A-12, with generator power swings shown in Figure A-13.

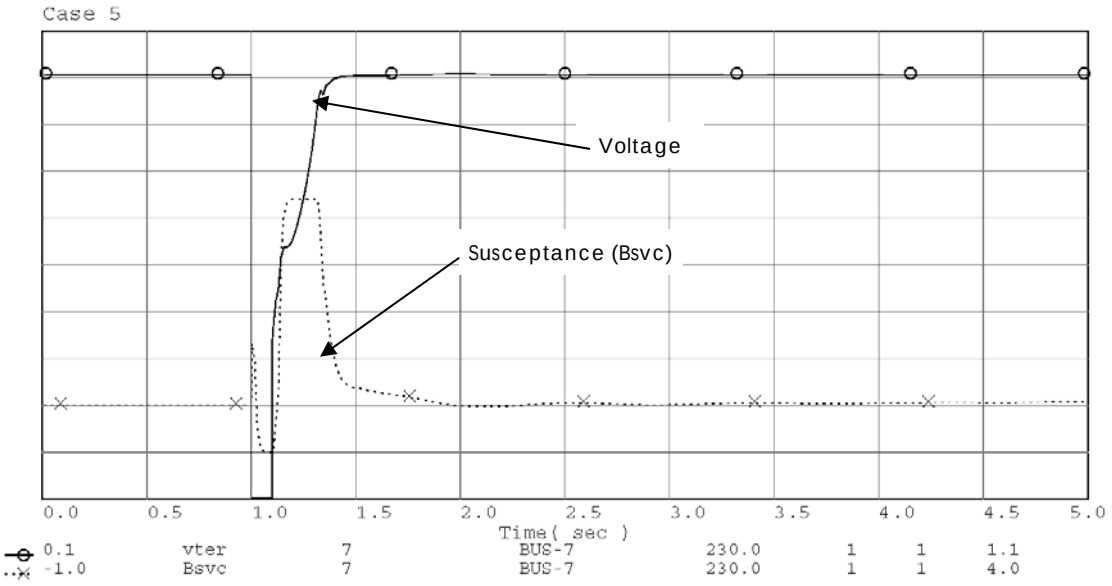


Figure A-12. Case 5 simulation result; voltage and susceptance.

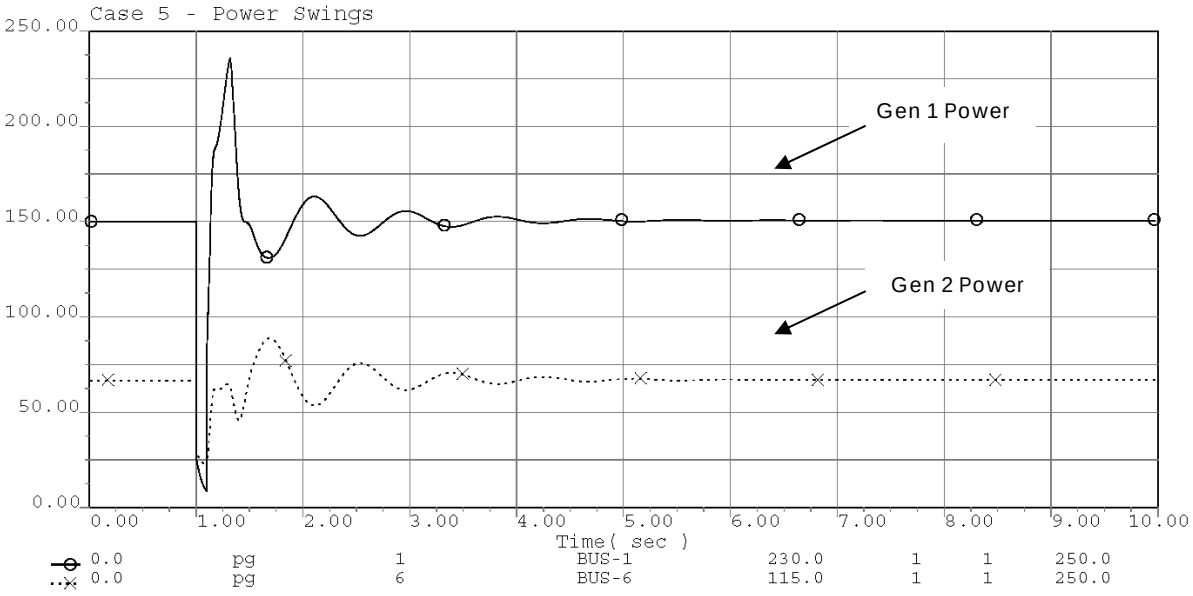


Figure A-13. Case 5 simulation result; power swings.

Case 6 – 2% Step Change

Case 6 demonstrates the generic SVC model's response to a 2% step change (increase) at 1 second in the simulation (slope=0.02).

The step change was implemented by adding the following EPCL code to the generic SVC model code:

```
@err = @vref - @vcomp
    if (dypar[0].time >= 1.0) /* DJS CHANGE FOR STEP RESPONSE */
   @err = @vref - @vcomp + 0.02 /* DJS CHANGE FOR STEP RESPONSE */
    endif  /* DJS CHANGE FOR STEP RESPONSE */
```

Regulated bus voltage and SVC susceptance are shown in Figure A-14.

(model filename: Generic_SVC_c2.p)

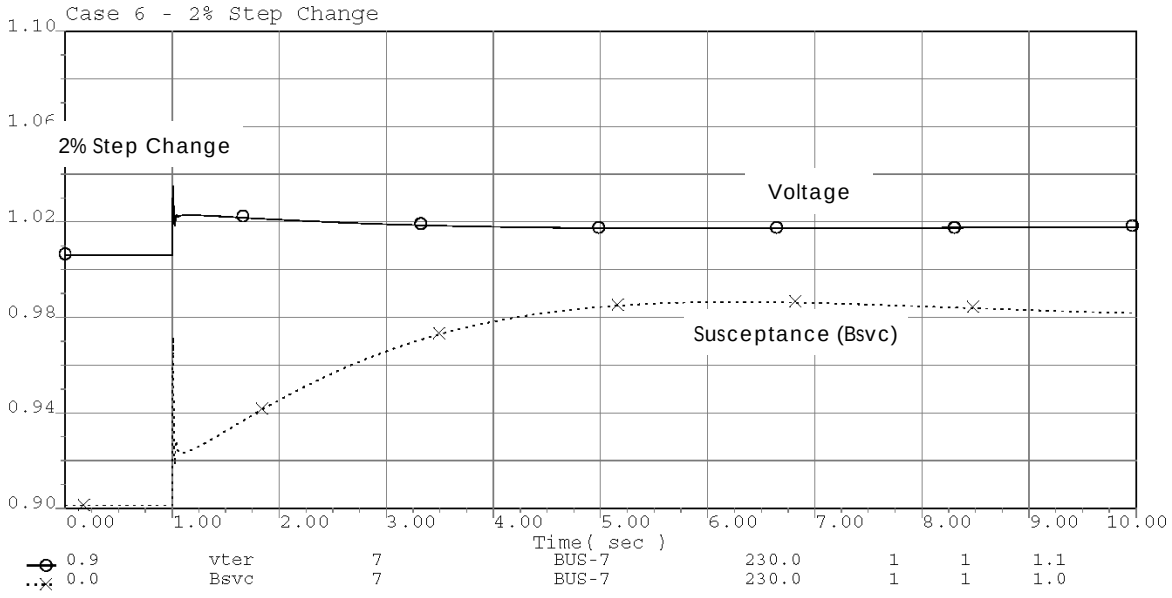


Figure A-14. Case 6 simulation result; voltage and susceptance.

Case 6 through 6e – Slope Variation

Case 6 through 6e illustrates the impact of varying the slope reactance (droop) from 0.01 to 0.1 for a 2% step change (increase) at 1 second in the simulation.

A comparison of regulated bus voltage for each slope variation is shown in Figure A-15.

(model filename: Generic_SVC_c2.p)

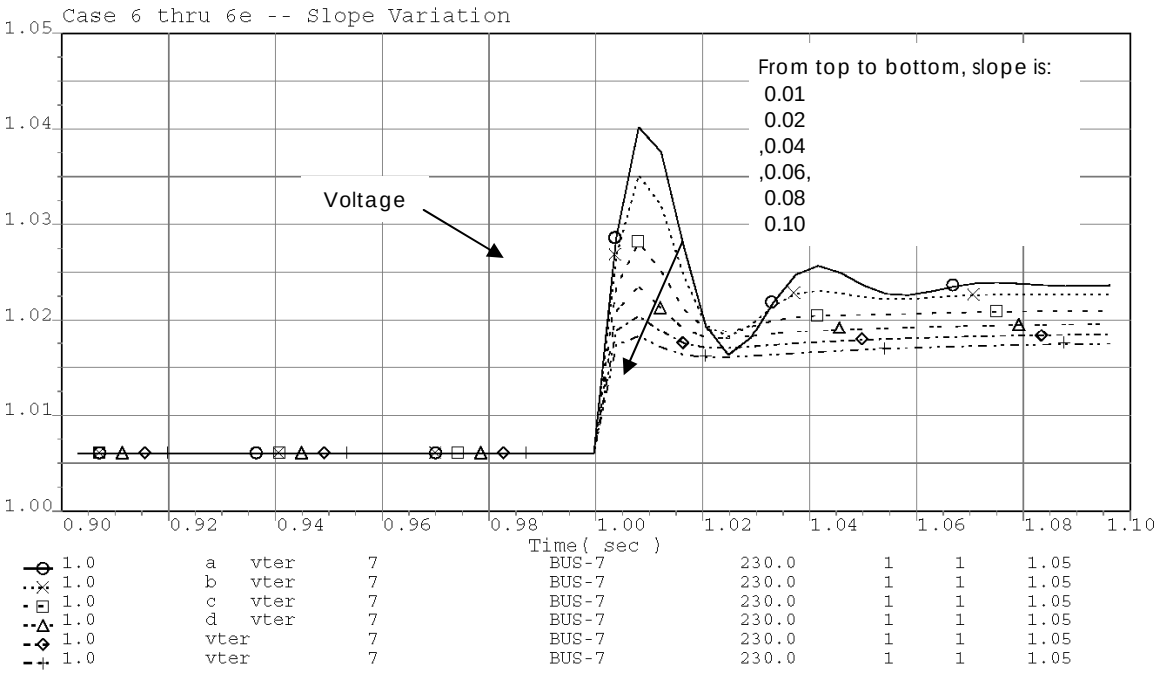


Figure A-15. Impact of slope variation on voltage response.

Case 7 – 2% Step Change and Vary Kpv/Kiv

Case 7 and Case 7a demonstrates the generic SVC model's response to a 2% step change (increase) at 1 second in the simulation with the proportional and integral gains of the voltage regulator increased.

- Kpv increased from 50 to 100 (Case 7)
- Kiv increased from 250 to 500 (Case 7a)

The result was then compared to Case 6, and is shown in Figure A-16 and Figure A-17.

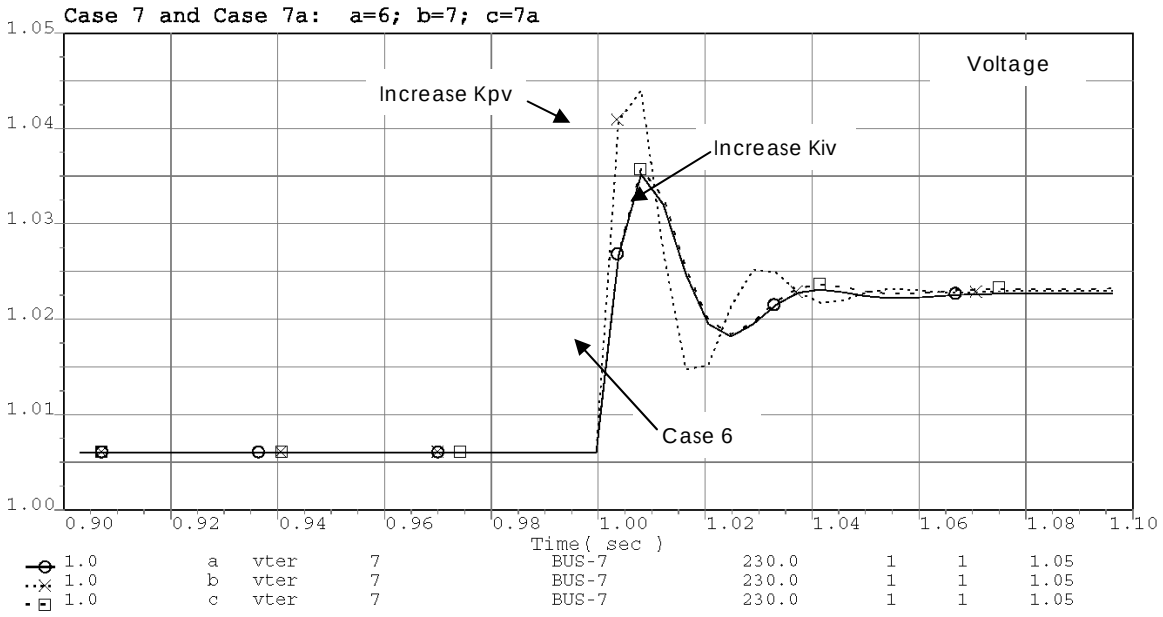


Figure A-16. Case 7 simulation result compared to Case 6; voltage.

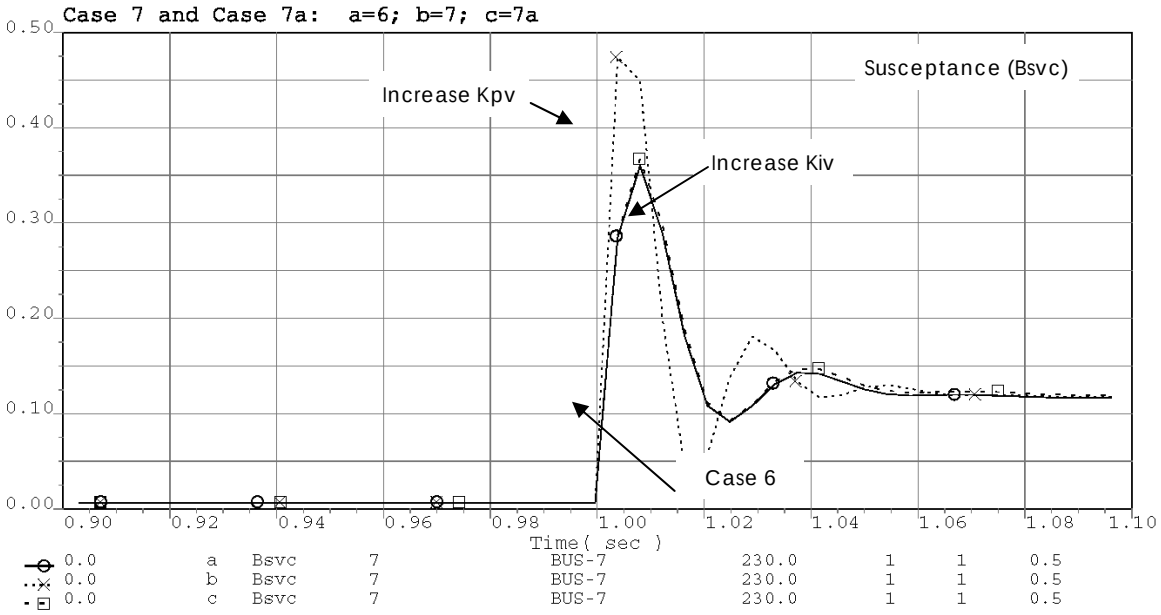


Figure A-17. Case 7 simulation result compared to Case 6; susceptance.

Case 8 – 2% Step Change and Vary Tc1/Tb1

Figure 8a and Figure 8b demonstrates the generic SVC model's response to a 2% step change (increase) at 1 second in the simulation with the lead and lag voltage measurement time constant increased.

$$\frac{1 + sTc1}{1 + sTb1}$$

- Tb1 is 0.01, and Tc1 is zero (Case6)
- Tb1 is 0.01, and Tc1 increased from 0 to 0.05 (Case 8)
- Tb1 increased from 0.01 to 0.08, and Tc1 is zero (Case 8a)

The result was then compared to Case 6, and is shown in Figure A-18 and Figure A-19.

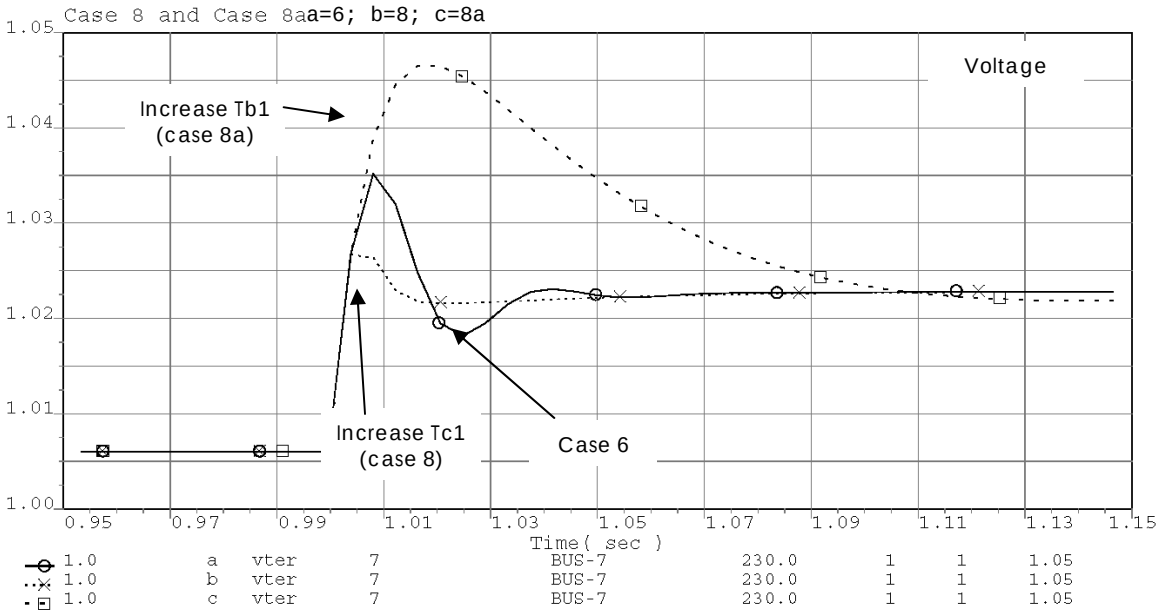


Figure A-18. Case 8 simulation result compared to Case 6; voltage.

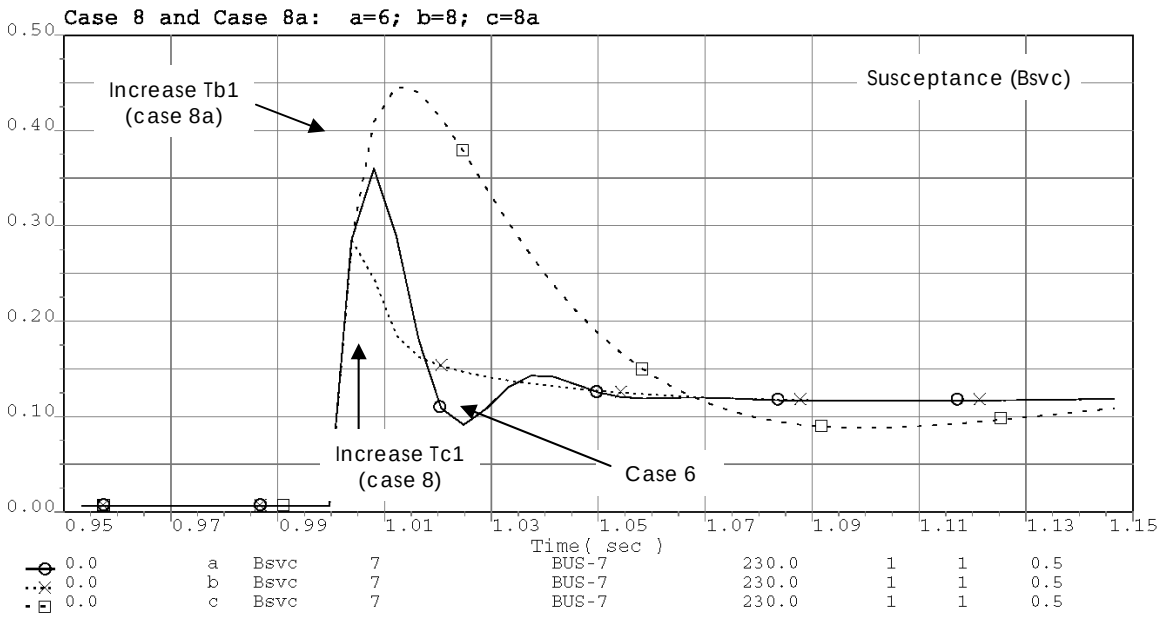


Figure A-19. Case 8 simulation result compared to Case 6; susceptance.

Case 9 – 2% Step Change and Vary Tc2/Tb2

Case 9 and Case 9a demonstrates the generic SVC model's response to a 2% step change (increase) at 1 second in the simulation with the lead and lag transient gain time constants measurement time constant increased.

$$\frac{1 + sTc2}{1 + sTb2}$$

- Tb2 is zero, and Tc2 is zero (Case6)
- Tb2 increased from 0 to 0.05, and Tc2 increased from 0 to 0.10 (Case 9)
- Tb2 increased from 0 to 0.05, and Tc2 is zero (Case 9a)

The result was then compared to Case 6, and is shown in Figure A-20 and Figure A-21.

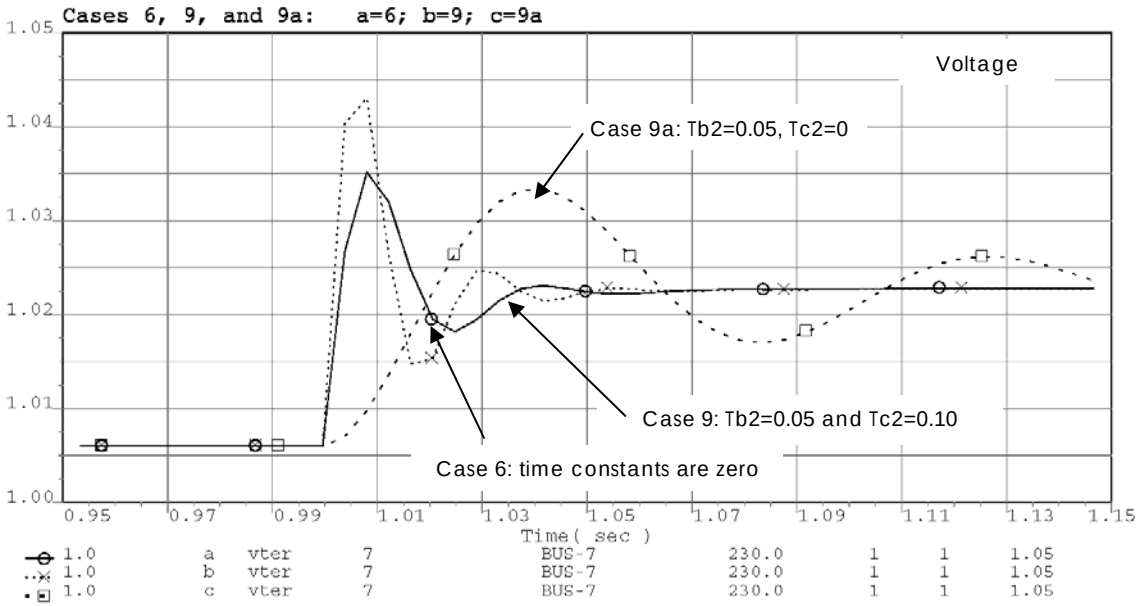


Figure A-20. Case 9 and 9a simulation results compared to Case 6; voltage.

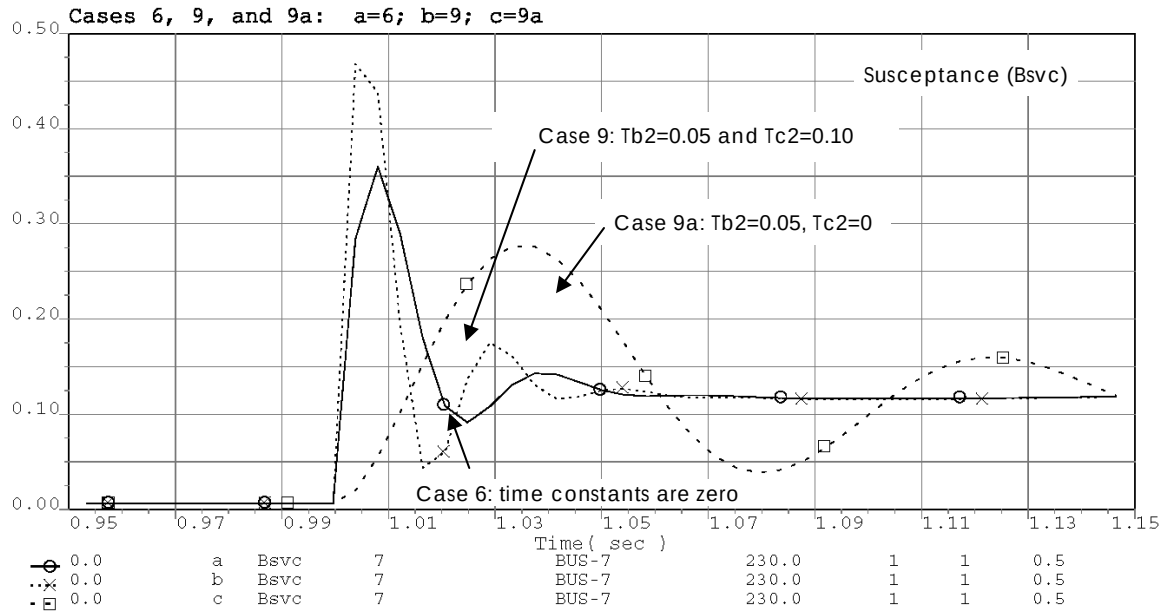
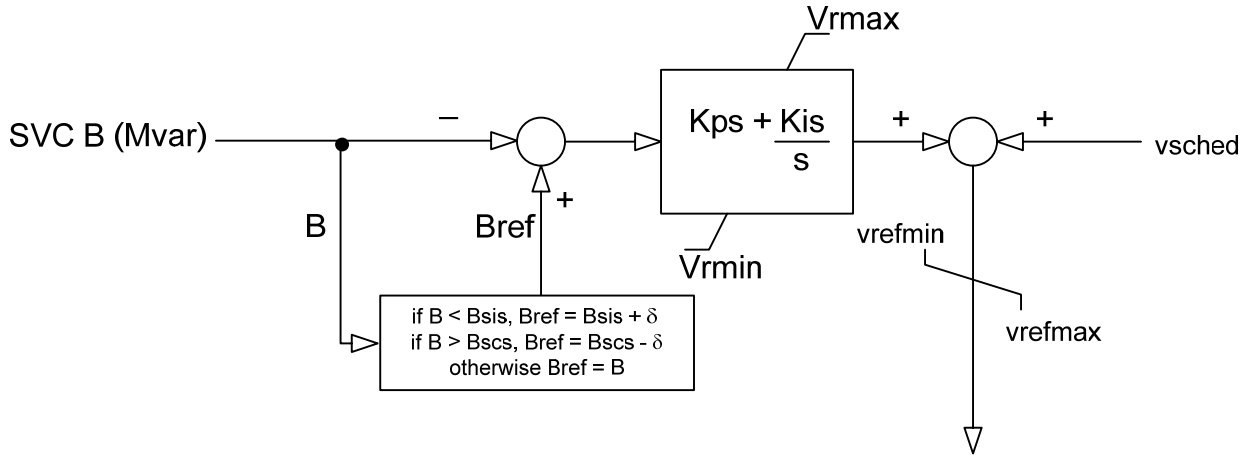


Figure A-21. Case 9 and 9a simulation results compared to Case 6; susceptance.

Case 10 – Step Change and With Slow Susceptance Control

Case 10 demonstrates the generic SVC model's response to a 2% step change (increase) at 1 second in the simulation with the slow susceptance control activated. The slow susceptance control loop shown below should work to reduce the SVC's output to within +/- 10 Mvar for this simulation case.



- Vrmin and Vrmax were change from zero to -/+ 0.5
- Bscs and Bsis were set to +10 Mvar and -10 Mvar

The result of Case 10 was then compared to Case 6, this is shown in Figure A-22.

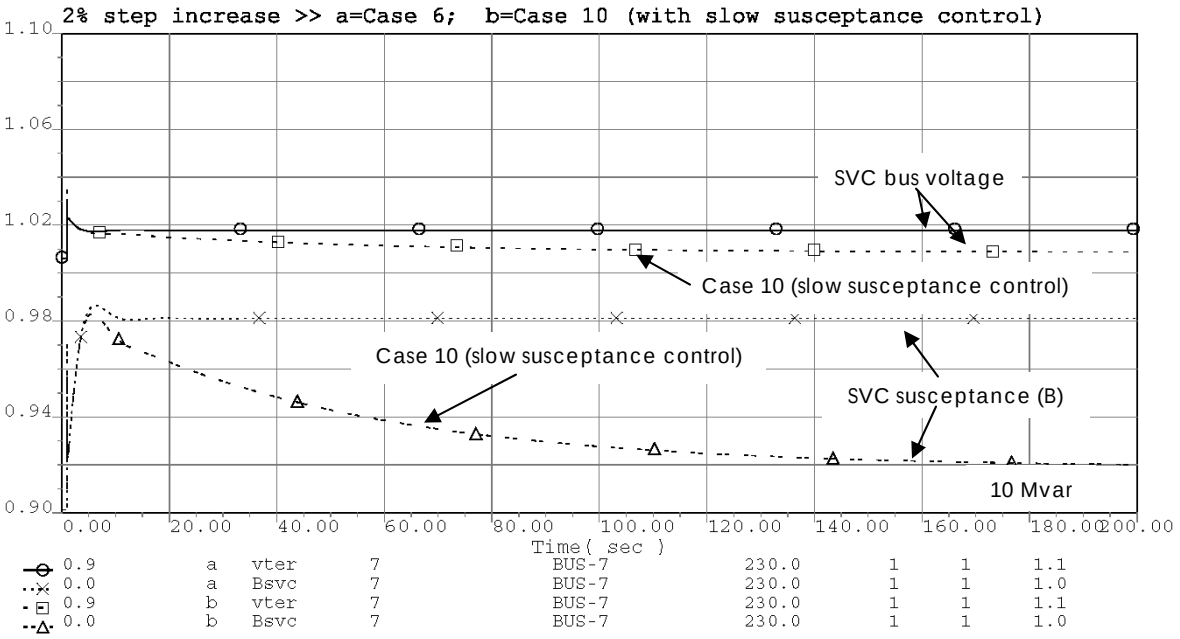


Figure A-22. Case 10 simulation result

Case 11 – Test Overvoltage Trip

Case 11 demonstrates the generic SVC model's response and subsequent trip resulting from a voltage increase (switching on 30 Mvar capacitor) simulated at 1 second in the simulation.

- OV1 was decreased from 1.3 to 1.03
- Bmin was decreased from -0.50 pu to -0.05

The SVC was tripped by OV1 threshold being exceeded for the time delay specified in parameter OVtm1, as shown in Figure A-23.

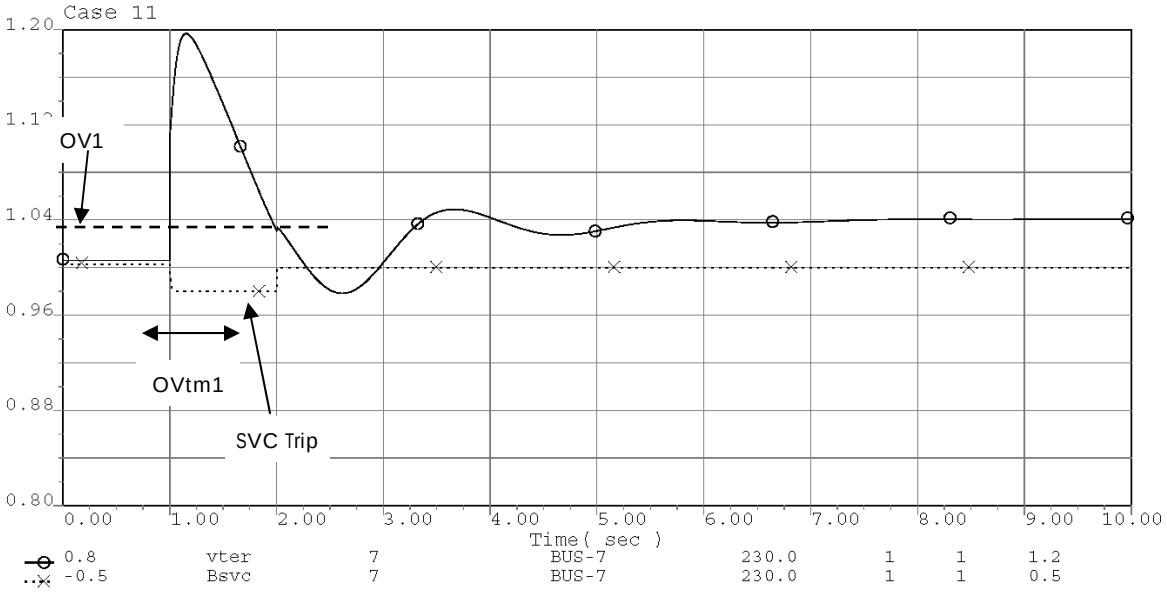


Figure A-23. Case 11 simulation result

Case 12 – Test Deadband Control

Case 12 demonstrates the generic SVC model's response to intentional variations in the regulated bus by MSS capacitor switching with the voltage deadband control activated.

This case was re-simulated with the voltage deadband turned off.

The voltage was varied with the following capacitor switching operation:

- 0 sec – no capacitors on
- 1-5 sec – two capacitors switched on (total 2x30 Mvar)
- 5-10 sec – one capacitor switched on (total 3x30 Mvar)
- 10-15 sec – two capacitors switched off (total 1x30 Mvar)
- 15-20 sec – one capacitor switched on (total 2x30 Mvar)

With the deadband control activated, the following control parameters were applied:

- CONT_Vdbd1 was set at 0.04
- CONT_Vdbd2 was set at 0.02
- CONT_Vdbd was set at 1 second

Figure A-24 illustrates the operation of the deadband control function, with Figure A-25 illustrating the same case without the deadband control activated. Figures A-26 and A-27 compare the two cases.

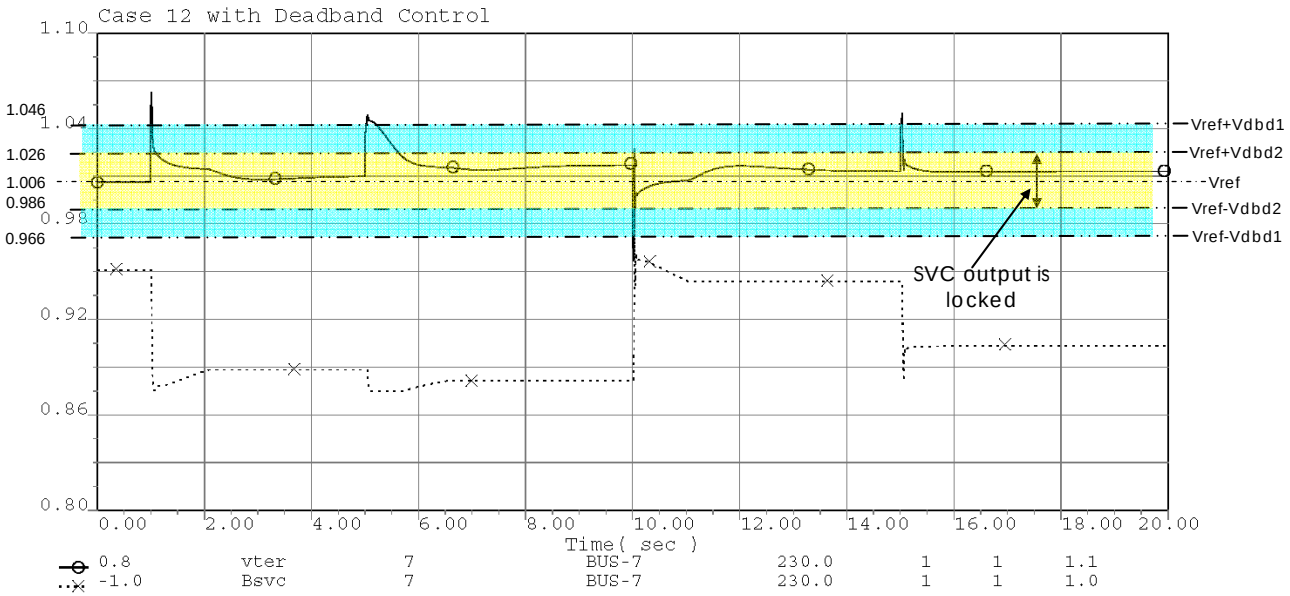


Figure A-24. Case 12 simulation result – with deadband control activated

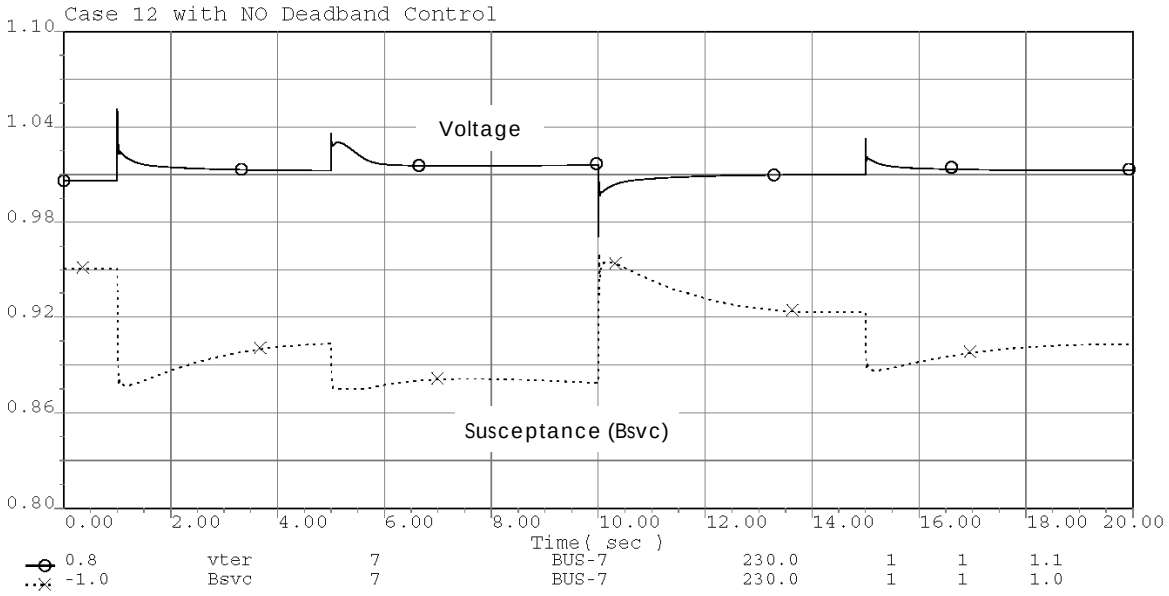


Figure A-25. Case 12 simulation result – <u>without</u> deadband control activated

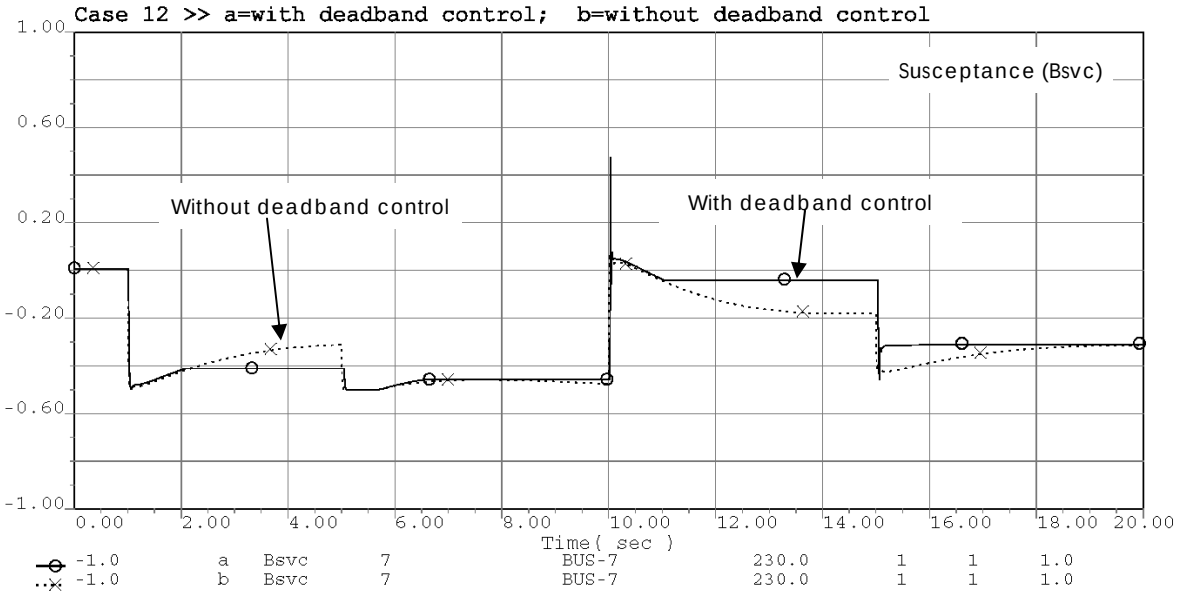


Figure A-26. Case 12 – <u>comparing Bsvc with and without deadband control.</u>

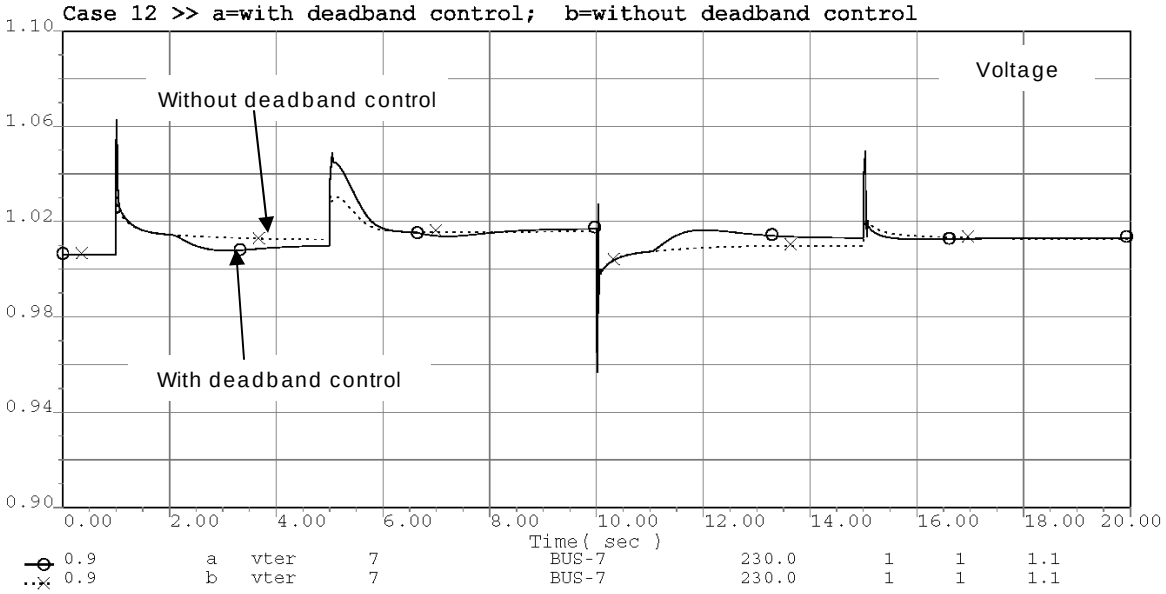


Figure A-27. Case 12 – comparing regulated bus voltage with and without deadband control

Case 13 – Test Non-Linear Slope

For Case 13, the simulation from Case 12 was rerun with the non-linear slope function activated.

With the non-linear control activated, the following control parameters were applied:

- flag1 set to 1
- CONT_Xc1 was set at 0.02
- CONT_Xc2 was set at 0.10
- CONT_Xc3 was set at 0.02
- CONT_Vup was set at 1.05
- CONT_Vlow was set at 0.95

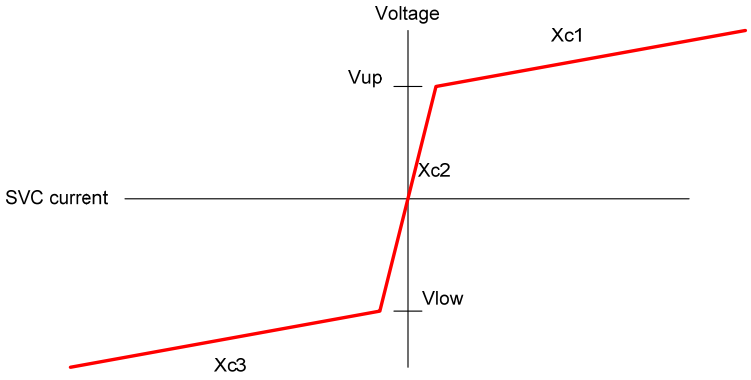


Figure A-28 illustrates the operation of the non-linear slope control function, with Figures A-29 and A-30 illustrating the comparison between Case 13 and Case 12 (without deadband control)

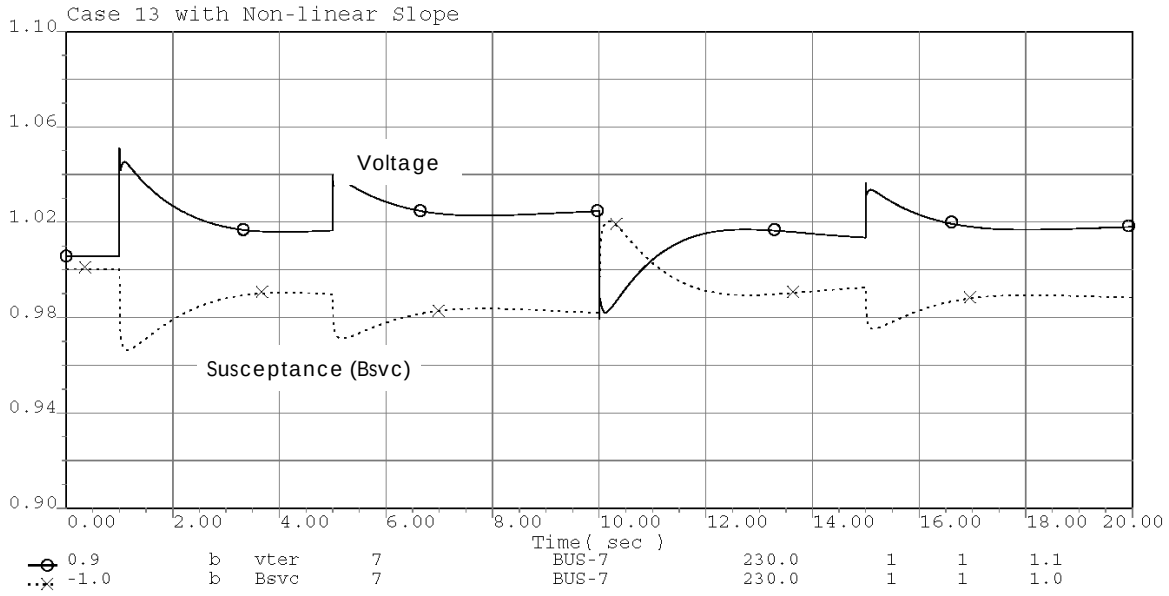


Figure A-28. Case 13 simulation result with non-linear slope activated.

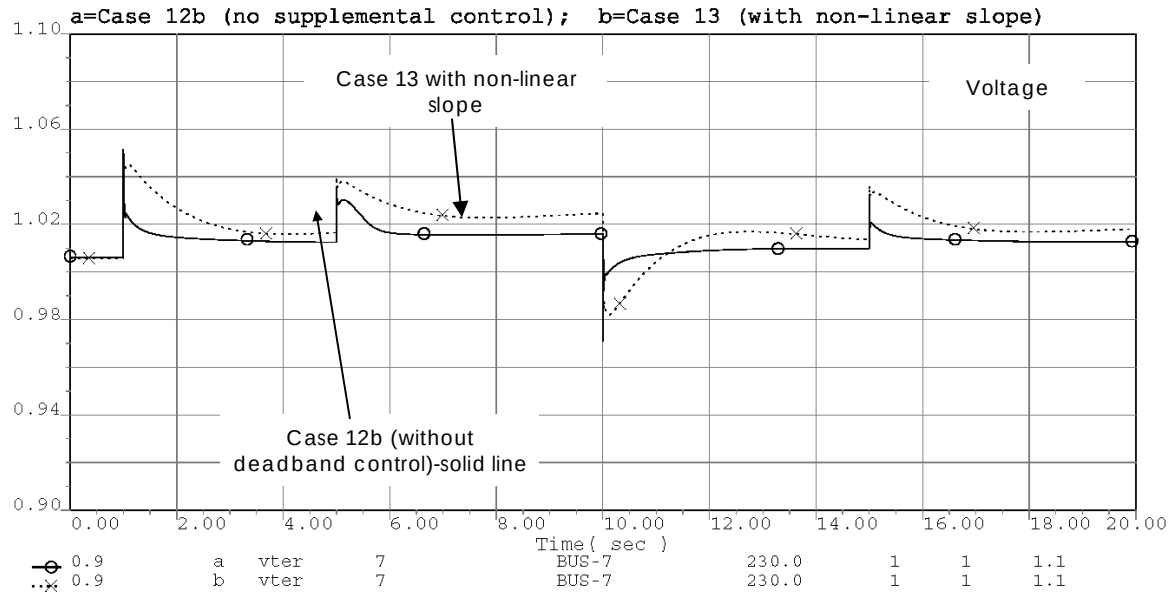


Figure A-29. Voltage for Case 13 simulation compared to Case 12b (with no deadband control).

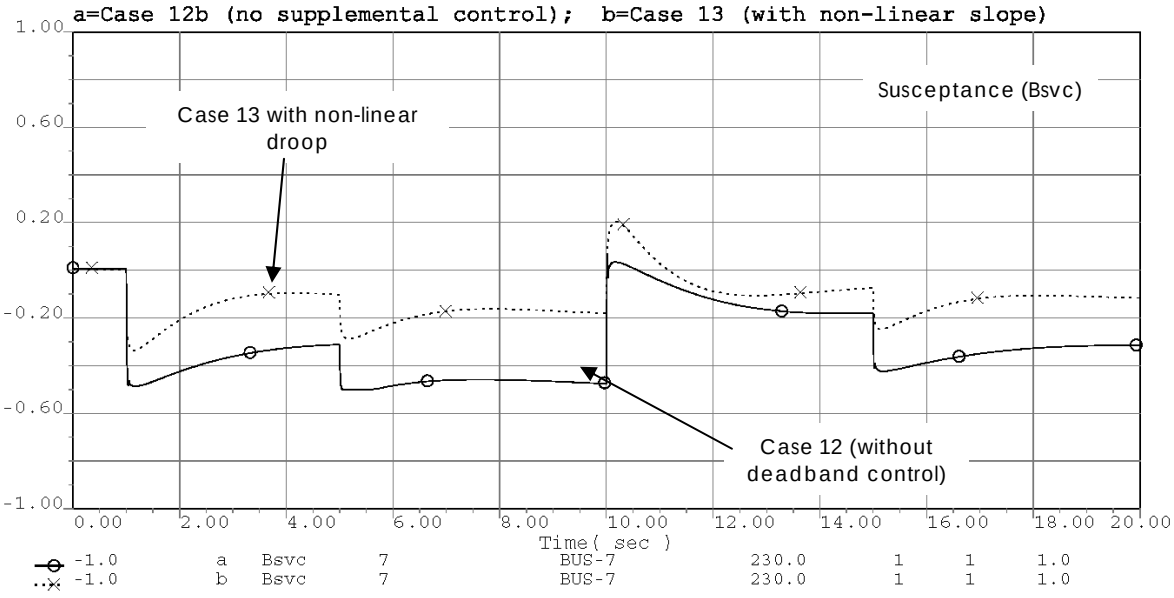


Figure A-30. Susceptance for Case 13 simulation compared to Case 12b (with no deadband control).

Case 14 – Test MSS Switching

Case 14 demonstrates the generic SVC model's capability to mechanically-switched shunt (MSS) devices such as capacitor banks based on reactive power output of the SVC. Intentional voltage variations were implemented to the regulated bus by changing Vsch through the dynamic simulation. There are four, 30 Mvar MSS devices available for switching in this simulation case.

The voltage was varied with the following capacitor switching operation:

- 0 sec – Vsch = 1.006 pu
- 1-20 sec – Vsch = 1.026 pu
- 20-40 sec – Vsch = 1.05 pu
- 40-60 sec – Vsch = 1.026 pu
- 60-80 sec – Vsch = 1.006 pu

With the MSS switching activated, the following control parameters were applied:

- flag1 = 1
- Blcs was set at 40 Mvar (larger capacitive threshold for switching MSSs)
- Bscs was set at 20 Mvar (smaller capacitive threshold for switching MSSs)
- Bsis was set at -20 Mvar (smaller inductive threshold for switching MSSs)
- Blis was set at -40 Mvar (larger inductive threshold for switching MSSs)
- Tdelay1 was set to 0.5 seconds (delay for larger threshold)
- Tdelay2 was set to 3 seconds (delay for smaller threshold)

Figure A-31 illustrates the operation of the MSSs, including the scheduled voltage and the SVC's susceptance.

- MSS 1 AT SVC SWITCHED IN AT TIME:4.821683
- MSS 2 AT SVC SWITCHED IN AT TIME:8.761267
- MSS 3 AT SVC SWITCHED IN AT TIME:22.289391
- MSS 4 AT SVC SWITCHED IN AT TIME:24.385181
- MSS 1 AT SVC SWITCHED OUT AT TIME:44.671082
- MSS 2 AT SVC SWITCHED OUT AT TIME:62.373989
- MSS 3 AT SVC SWITCHED OUT AT TIME:65.495934

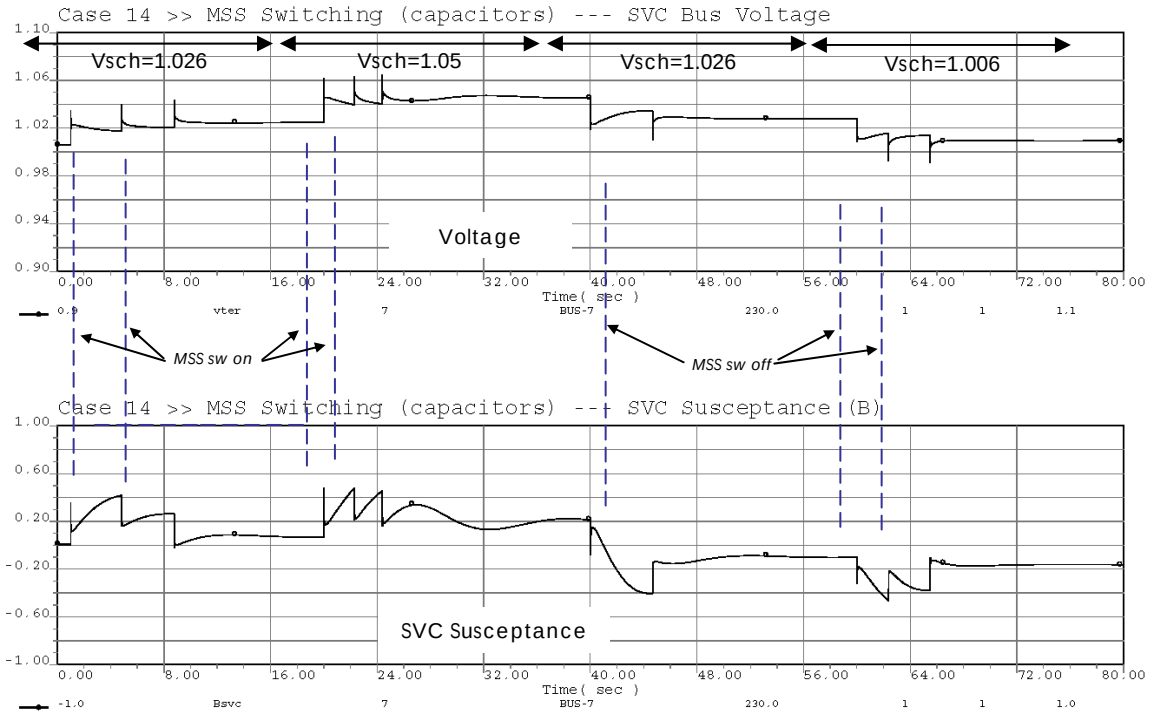


Figure A-31. Case 14 simulation result.

It was confirmed that once the MSS capacitors were switched in and out, they were prohibited from switching back in (within the time specified by input parameter @Tout)

Various combinations of deadband control, non-linear slope, and slow susceptance supplemental controls were attempted for dynamic simulations. Warnings and control disable actions were observed during initialization. Therefore, it has been confirmed that no combinations of these three supplemental controls can be implemented.

Case 14 was repeated with revised epcl code for the SVC Model to allow MSS switching of an inductor.

```
/********************/
/* MSS Logic Parm. */
/********************/
  @Blcs = 40.0          /* Larger threshold for switching MSSs                                  */
  @Bscs = 20.0          /* Smaller threshold for switching MSSs                                 */
  @Blis = --20.0        /* Smaller threshold for switching MSSs                                 */
  @Bsis = -40.0         /* Larger  threshold for switching MSSs                                 */
  @Tmssbrk = 0.10       /* Time for MSS breaker to operate - typically ignore                   */
  @tdelay1 = 0.50       /* Time delay for larger threshold                                      */
  @tdelay2 = 3.0        /* Time delay for smaller threshold (should be much larger than tdelay1) */
  @Tout = 300.0         /* Time cap. bank should be out before switching back in                */
```

Data from log file depicting the time when MSSs were switched in and out in the simulation:

- MSC 1 AT SVC SWITCHED IN AT TIME:5.283582
- MSC 2 AT SVC SWITCHED IN AT TIME:10.810758
- MSC 3 AT SVC SWITCHED IN AT TIME:23.372885
- MSC 1 AT SVC SWITCHED OUT AT TIME:42.02079
- MSC 2 AT SVC SWITCHED OUT AT TIME:42.860786
- MSC 3 AT SVC SWITCHED OUT AT TIME:43.919182
- MSR 4 AT SVC SWITCHED IN AT TIME:60.605698
- MSCs AT SVC ARE ALL OUT-OF-SERVICE OR NO MSRs TO SWITCH IN.
- MSR 4 AT SVC SWITCHED OUT AT TIME:86.182686

Based on the simulation plot in Figure A-32, it was confirmed that both MSS capacitors and reactors were switched in and out as defined by the SVC model input parameters.

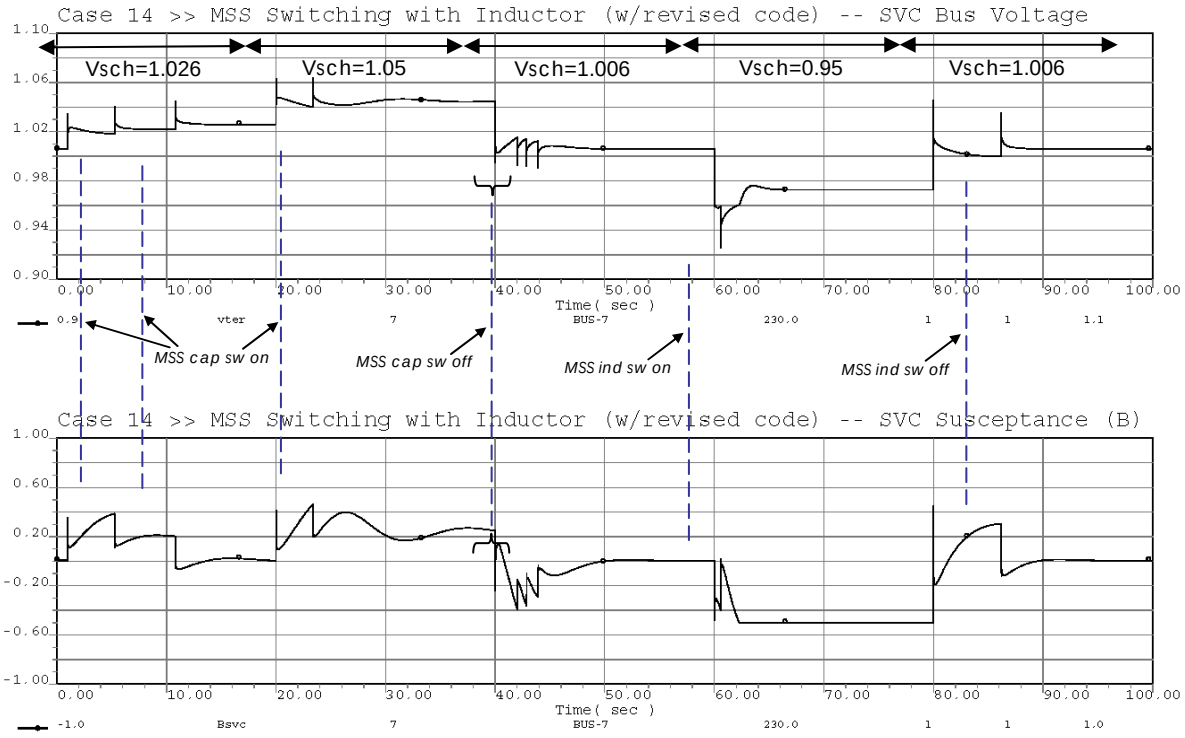


Figure A-32. Case 14 simulation result with Inductor switching.

Case 15 – Step Change and Vary Firing Transport Delay (T2)

Case 15 demonstrates the generic SVC model's response to a 2% step change (increase) at 1 second in the simulation with the valve firing transport delay increased.

- T2 increased from 0.01 to 0.05

The result was then compared to Case 6 in Figure A-33 and Figure A-34.

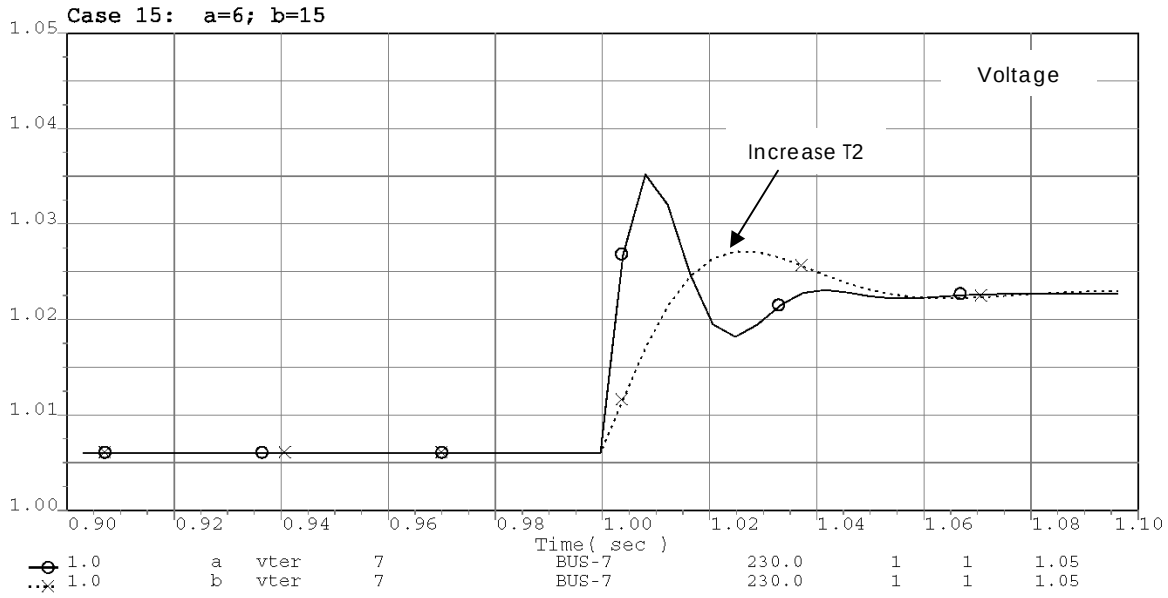


Figure A-33. Case 15 simulation result

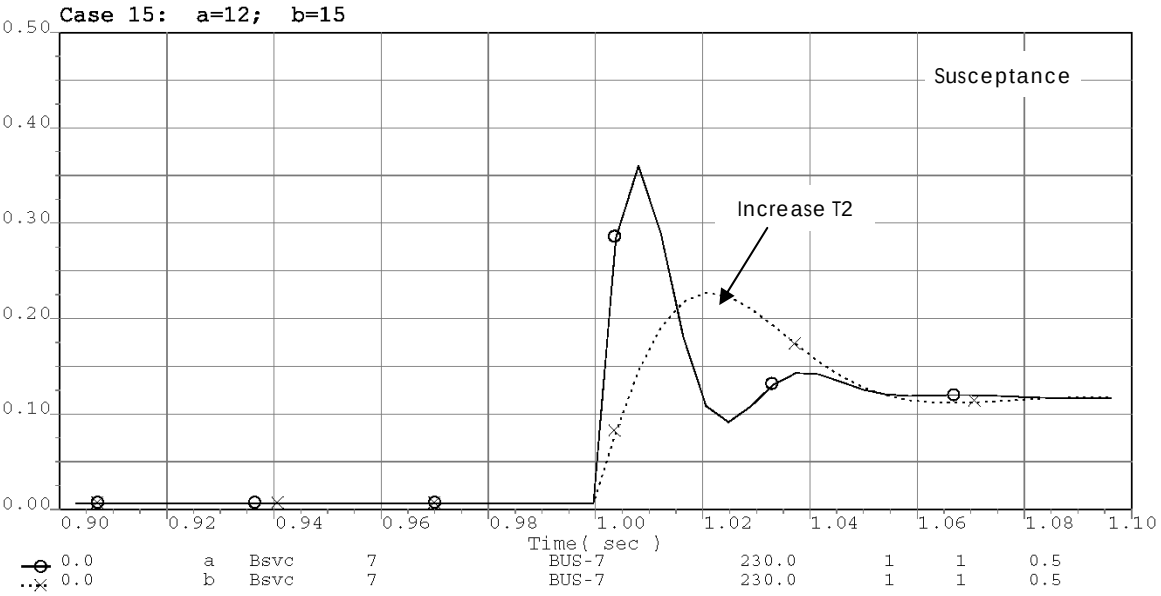


Figure A-34. Case 15 simulation result

Case 16 – Power Oscillation Damping (POD) Control

An example of this test was shown in the main text of the report – see Figure 2-5.

Table A-2 - Model Parameter Input Parameters for Test Cases

Input Parameter Description		Parameter Name	Units	Case 1	case 1b	case 1c	Case 2	Case 3 Case 3a	Case 4	Case 5	Case 6	Case 6a	Case 6b	Case 6c	Case 6d	Case 6e	Case 7	Case 10	Case 11	Case 12a w/deadband	Case 12b w/out deadband	Case 13	Case 13_r1	Case 14	Case 15
Max. cap. limit during undervoltage strategy (assumed filter size)	@	UVSBmax	pu (100 MVA)	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Under voltage setting 1	@	UV1	pu	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Under voltage setting 2	@	UV2	pu	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
Under voltage trip setting	@	UVT	pu	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Over voltage setting 1	@	OV1	pu	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.03	1.3	1.3	1.3	1.3	1.3	1.3
Over voltage setting 2	@	OV2	pu	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5
Under voltage trip time 1	@	UVtm1	sec	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Under voltage trip time 2	@	UVtm2	sec	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
Over voltage trip time 1	@	OVtm1	sec	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Over voltage trip time 2	@	OVtm2	sec	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
Bus number for MSSs	@	mscbuss		3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
Id of MSSs	@	mscid1		"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"	"c1"
Id of MSSs	@	mscid2		"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"	"c2"
Id of MSSs	@	mscid3		"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"	"c3"
Id of MSSs	@	mscid4		"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"	"c4"
0 - no MSS switching; 1 - MSS switching on Q (MVAr)	@	flag1		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0 - linear droop; 1 - non-linear droop (piecewise linear)	@	flag2		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
Slope/droop (for flag2 = 0, Xc1 is the droop)	@	CONT_Xc1		0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.01	0.04	0.06	0.08	0.1	0.02	0.02	0.02	0.02	0.02	0.02	0.1	0.02	0.02
Slope/droop	@	CONT_Xc2		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.1	0.02	0	0
Slope/droop	@	CONT_Xc3		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.02	0.02	0	0
Upper voltage break-point for non-linear Slope/droop	@	CONT_Vup		1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.05	1.05	0	1.1
Lower voltage break-point for non-linear Slope/droop	@	CONT_Vlow		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.95	0.95	0	0
Voltage measurment lead time constant	@	CONT_Tc1	sec	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Voltage measurment lag time constant	@	CONT_Tb1	sec	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
lead time constant	@	CONT_Tc2		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
lag time constant	@	CONT_Tb2		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Proportional gain	@	CONT_Kpv		50	50	50	50	50	50	50	50	50	50	50	50	50	100	50	50	50	50	50	50	50	50
Integral gain	@	CONT_Kiv		250	250	250	250	250	250	250	250	250	250	250	250	250	250	250	250	250	250	250	250	250	250
Voltage error max.	@	CONT_vemax	pu	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Voltage error min.	@	CONT_vemin	pu	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5
Thyristor firing sequence control delay CAN'T BE ZERO	@	CONT_T2	sec	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.05
Short-term max. suceptance of SVC (short-term rating)	@	CONT_Bshrt	pu (100 MVA)	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Max. suceptance of SVC (continuous rating)	@	CONT_Bmax	pu (100 MVA)	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Min. suceptance of SVC	@	CONT_Bmin	pu (100 MVA)	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.05	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5
Duration of short-term rating	@	CONT_Tshrt	sec	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
Proportional gain of slow suceptance control	@	CONT_Kps		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Integral gain of slow suceptance control	@	CONT_Kis		0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001	0.00001
Max. output of slow suceptance control	@	CONT_Vrmax	pu	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.5	0	0	0	0	0	0	0
Min. output of slow suceptance control	@	CONT_Vrmin	pu	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-0.5	0	0	0	0	0	0	0
Steady-state Voltage deadband; SVC is inactive between Vref+Vdbd1 to Vref-Vdbd1	@	CONT_Vdbd1	pu	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.04	0	0	0	0	0
Inner deadband; i.e. when SVC goes outside of Vdbd1, it must come back within	@	CONT_Vdbd2	pu	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.02	0	0	0	0	0
Vdbd2 for Tdbd seconds in order to be locked again	@	CONT_Vdbd	pu	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Larger threshold for switching MSSs	@	Bin1	Mvar	20	20	20	20	20	20	20	20	20	20	20	20	20	20	0	20	20	20	20	20	40	20
Smaller threshold for switching MSSs	@	Bin2	Mvar	70	70	70	70	70	70	70	70	70	70	70	70	70	70	10	70	70	70	70	70	20	70
Larger threshold for switching MSSs	@	Bout1	Mvar	-40	-40	-40	-40	-40	-40	-40	-40	-40	-40	-40	-40	-40	-40	0	-40	-40	-40	-40	-40	-40	-40
Smaller threshold for switching MSSs	@	Bout2	Mvar	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-20	-10	-20	-20	-20	-20	-20	-20	-20
Time for MSS breaker to operate - typically ignore	@	Tmscbrk	sec	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Time delay for larger threshold	@	tdelay1	sec	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Time delay for smaller threshold (should be much larger than tdelay1)	@	tdelay2	sec	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	3	6
Time cap. bank should be out before switching back in	@	Tout	sec	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300

FOR REFERENCE ONLY – DYNAMIC DATA FILE (dyd) FOR THE TEST CASE

```
#
# DYNAMICS DATA CREATED FOR TESTING SVC MODEL -- FOR WECC SVC MODELING TASK FORCE --- June 2008
#
# DAN SULLIVAN, Mitsubishi Electric Power Products, Inc. (MEPPI)
# POUYAN POURBEIK, Electric Power Research Institute (EPRI)
#
#
smes1    7  "BUS-7 " 230.00 "1 " : #9 mva=100.0000  "Generic_SVC_c1.p" 3.0000  "rcomm" 0.0000 /
xcomm 0.0000  "cntrbus" 0.0000  "capbus" 0.0000  "kp_i" 0.0000  "ki_i" 0.0000  "tdelay_lpk" 0.0000 /
tdelay_p 0.0000  "Vthr_lpk" 0.0000  "Imin" 0.0000  "Imax" 0.0000  "ImPk" 0.0000  "T_ImPk" 0.0000 /
T_Im_rmp 0.0000  "V_hg_p" 0.0000  "V_lw_p" 0.0000  "pk_mw" 0.0000  "rate_p" 0.0000  "tdisc" 0.0000 /
delay_c 0.0000  "B_cap" 0.0000  "V_cap_off" 0.0000  "vref_lw" 0.0000  "vref_hg" 0.0000  "accel" 0.0000
motorw   2  "BUS-2 " 230.00 "1 " : #9 mva=0.0000    0.400000   3.6000 0.170000 0.006800 0.530000 0.500000   2.0000 0.600000  30.0000 0.033330 0.600000 0.170000 0.0  10.0000 0.800000
motorw   4  "BUS-4 " 115.00 "1 " : #9 mva=0.0000    0.400000   3.6000 0.170000 0.006800 0.530000 0.500000   2.0000 0.600000  30.0000 0.033330 0.600000 0.170000 0.0  10.0000 0.800000
genrou   1  "BUS-1 "  230.00 "1 " : #9 mva=156.6000  4.8000 0.0330 0.4100 0.0700 /
 6.5000 0.0000 2.1400 2.0400 0.2400 0.5000 0.2300 /
 0.1900 0.1000 0.4000 0.0000 0.0000 0.0000 0.0000
exst4b   1  "BUS-1 "  230.00 "1 " : #9 0.020000   3.1500   3.1500 0.010000 1.000000 -0.870000 1.000000 0.0 1.000000 -0.870000 /
 0.0   6.5000 0.0 0.0 0.080000 0.0   8.0000
genrou   6  "BUS-6 "  115.00 "1 " : #9 mva=156.6000  4.8000 0.0330 0.4100 0.0700 /
 6.5000 0.0000 2.1400 2.0400 0.2400 0.5000 0.2300 /
 0.1900 0.1000 0.4000 0.0000 0.0000 0.0000 0.0000
exst4b   6  "BUS-6 "  115.00 "1 " : #9 0.020000   3.1500   3.1500 0.010000 1.000000 -0.870000 1.000000 0.0 1.000000 -0.870000 /
 0.0   6.5000 0.0 0.0 0.080000 0.0   8.0000
vmeta    1  "BUS-1 "  230.00 "1 " : #9 0.0 0.0
```

B. MODELING THE SVC AT THE TRANSMISSION LEVEL

There is often a discussion as it pertains to SVCs as to whether the device should be modeled at the transmission level or if the unit's transformer should be explicitly modeled and the SVC branches modeled explicitly at low voltage bus of the unit transformer.

This issue has been discussed and documented in the literature (e.g., [7]). None-the-less, it is felt that a brief summary of the subject is pertinent for clarity.

It should be noted that a typical specification of an SVC installation by a utility will specify the required SVC range at the transmission level bus (the high voltage side of the SVC coupling transformer – bus 1 in Figure B-1). Large SVC applications are primarily for transmission system voltage support, thus the equipment specification will be for require reactive support at the transmission voltage level. Furthermore, a typical specification will identify the range of steady-state voltages for which the full reactive capability of the SVC should be available continuously (e.g., from 0.9 to 1.1 pu voltage).

Furthermore, a typical SVC control system will actually control the unit's susceptance (B) as measured on the high voltage side of the coupling transformer.

Thus, vendors will optimize and design the combination of the SVC branches (TCR/TSC) and the coupling transformer to ensure that the effective SVC range at the transmission system voltage is as required and specified. In addition, the equipment is designed to sustain the higher voltage that will inherently occur at the secondary of the coupling transformer over the required continuous operating range of the SVC. Thus, the secondary voltage limitation control, the TCR and TSC current limiters will not typically come into play for momentary transients (e.g., faults and power swings) or during stead-state operation in the normal continuous range. As such, there is no value in modeling the coupling transformer explicitly and going to the complication of calculating the branch values at the secondary voltage level. Moreover, when performing studies to specify a potential SVC application, one can only truly assess what is needed at the transmission level – the sizing of the branches and coupling transformer are part of the optimization process of actual equipment design, best done by the equipment vendor.

As a simple exercise, consider the following example. Consider the two equivalent SVC models in Figure B-2. On the left hand side we have the model with the transformer explicitly modeled. In this case, the device total susceptance as seen at the high-voltage bus (Bus 1) is:

$$B_{svcmaxH} = \frac{1}{\frac{1}{j1.667} + j0.1} = j2.0 \text{ pu}$$

$B_{svcminH} = \frac{1}{\frac{1}{-j1.11} + j0.1}$ = -j1.0 pu

Thus, the two models are identical at the transmission level. Figure B-3 shows the VI characteristics of both models as seen at bus 1 (high voltage side). That is, I = V×B. This is further illustrated in Figure B-4 and B-5, which show the two cases simulated in GE PSLF™.

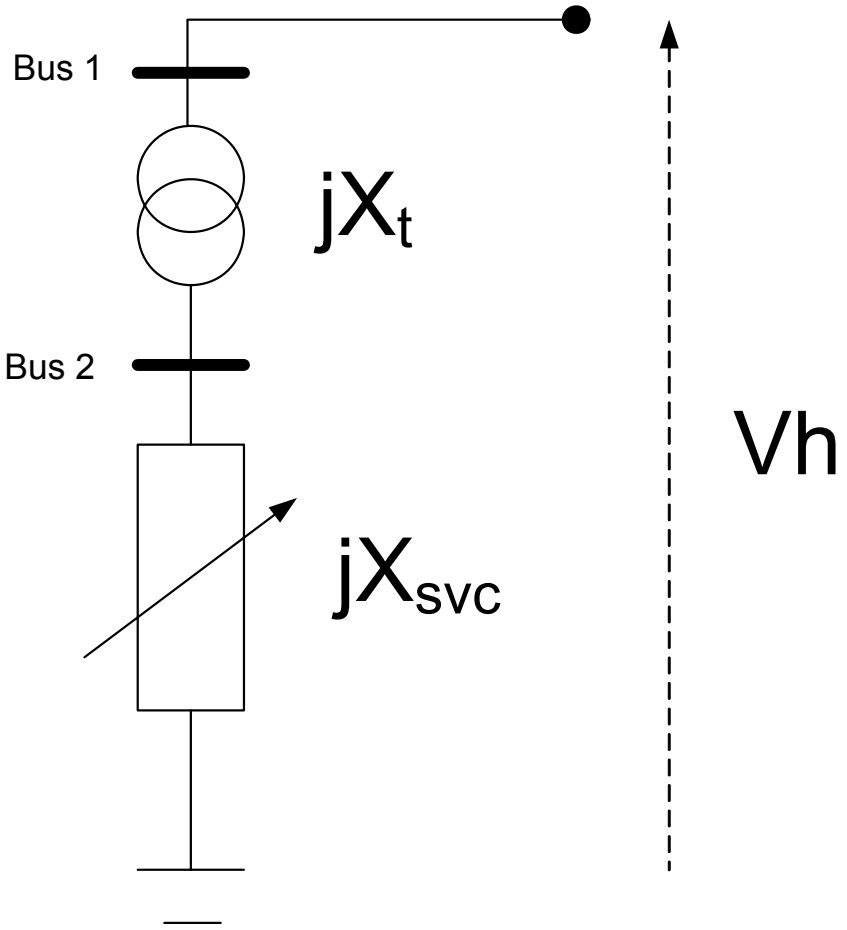


Figure B-1: SVC and coupling transformer.

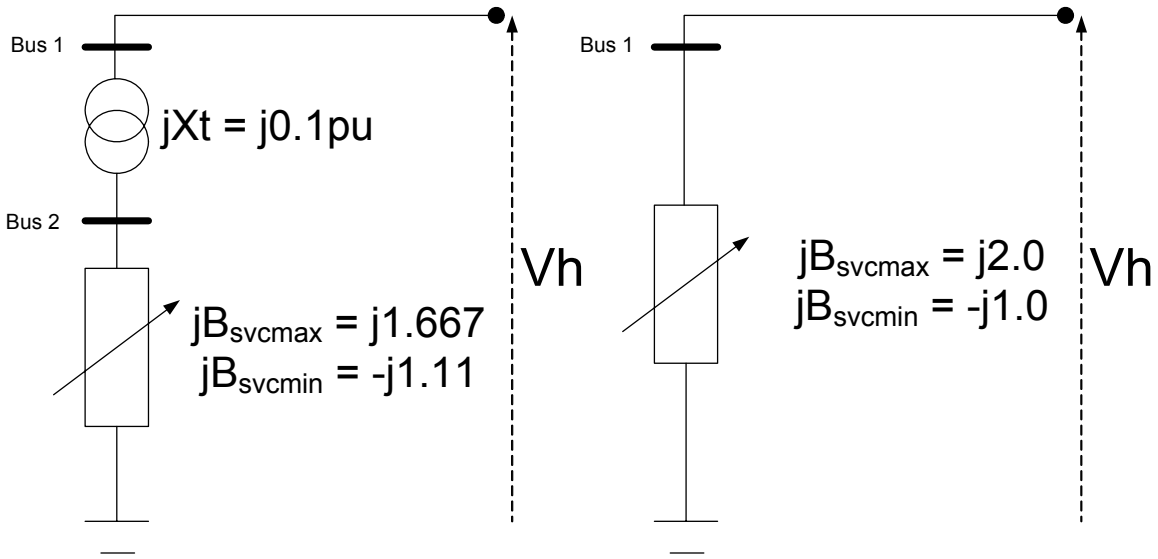


Figure B-2: SVC modeled with and without the coupling transformer.

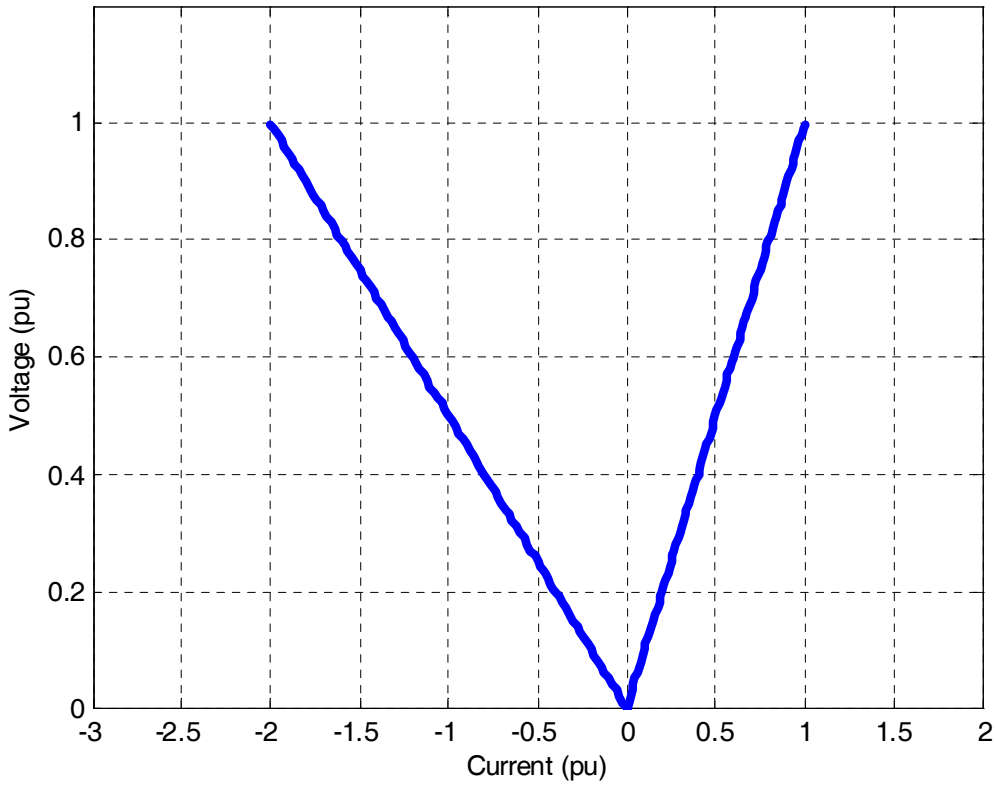
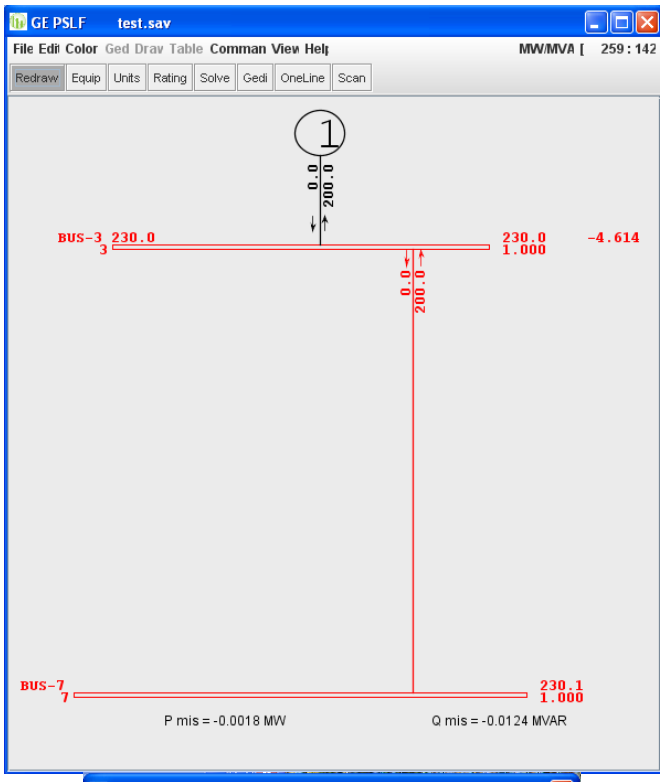


Figure B-3: SVC VI characteristic from 0 to 1 pu voltage (ideal case, not showing protection and under/overvoltage strategies).



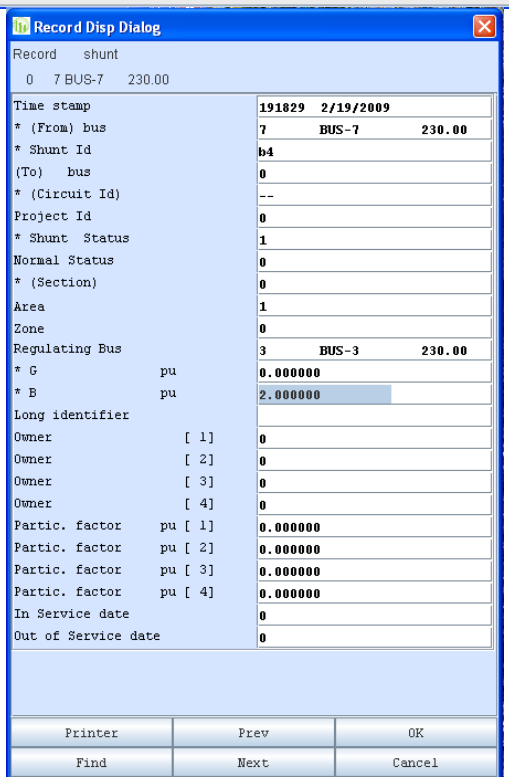


Figure B-4: High Side Model – Bmax = 2.0. Delivered Q at 1 pu voltage at 230 kV is 200 Mvar (see top figure; note line between bus 7, where SVC is located, and bus 3 is negligible, it has only been added to separate the buses)

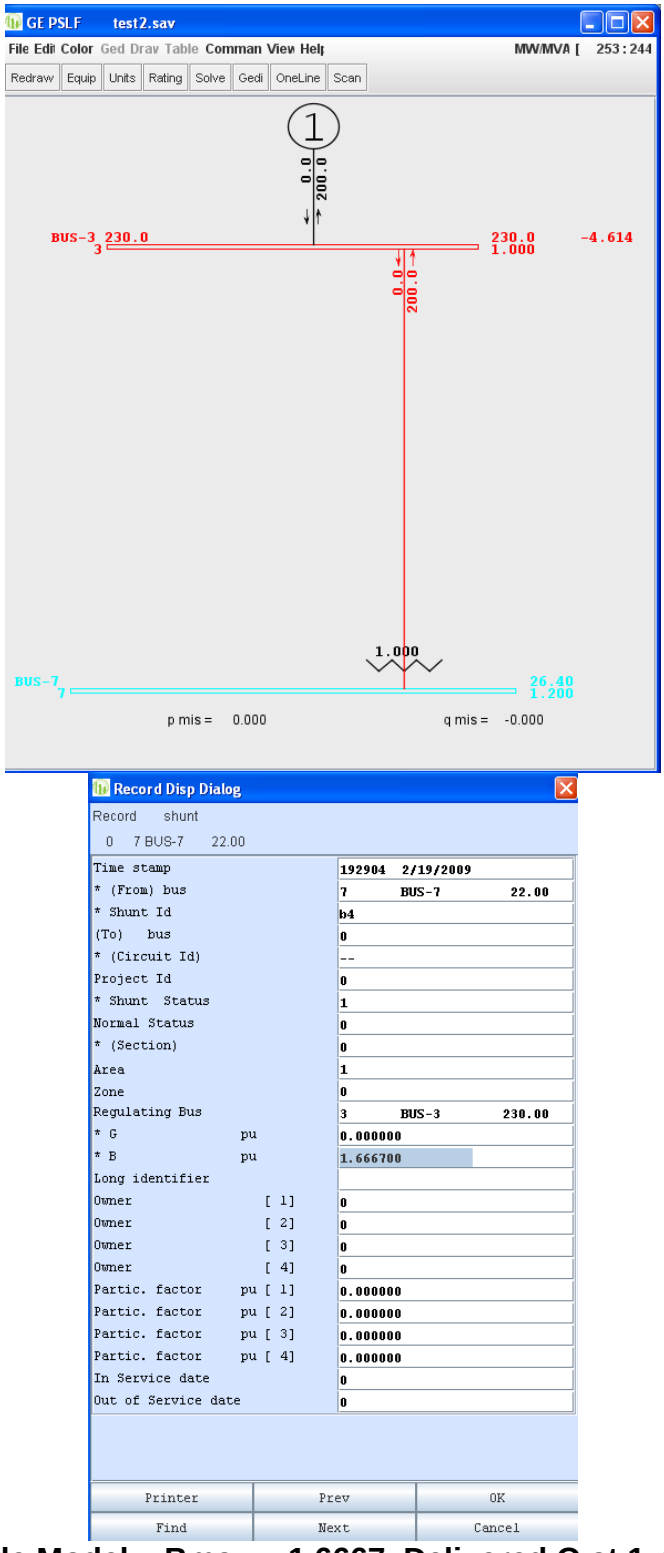
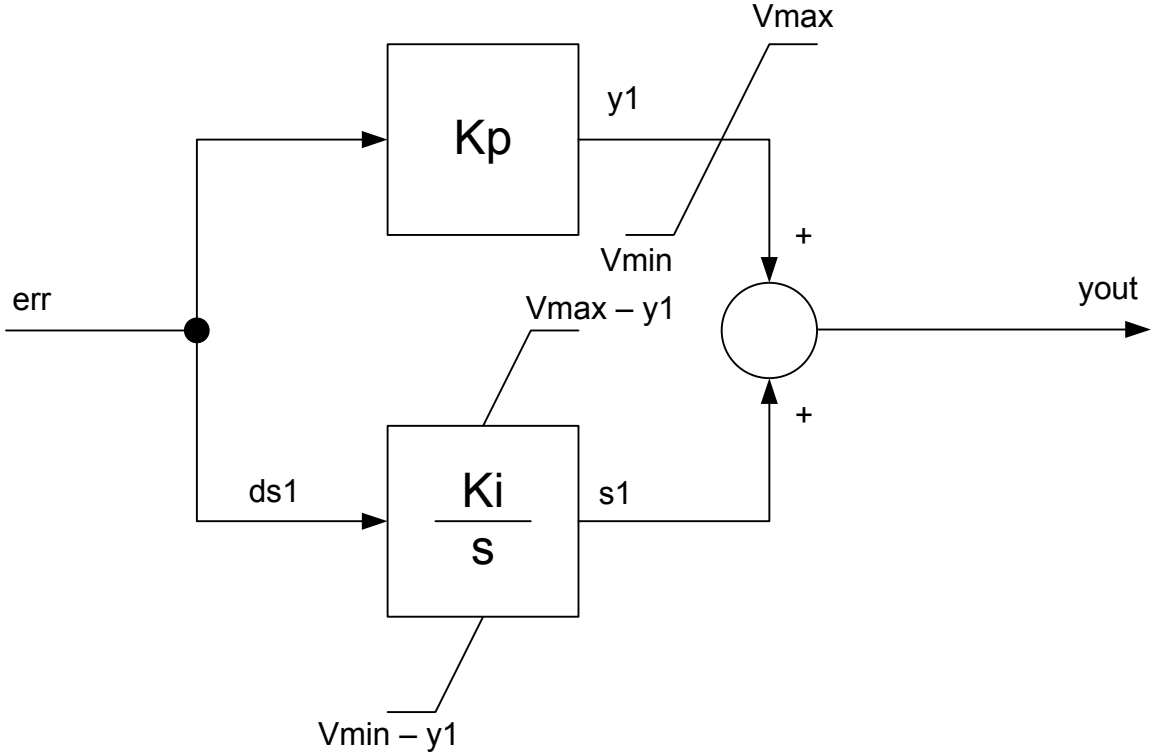


Figure B-5: Low Side Model – Bmax = 1.6667. Delivered Q at 1 pu voltage at 230 kV is 200 Mvar (see top figure; note 10%, on 100 MVA, transformer modeled from bus 7, where SVC is located at).

C. NON-WINDUP INTEGRATOR

The non-windup integrators in the models have been implemented as follows:




```
y1 = Kp × err
if (y1 > Vmax)
        y1 = Vmax
elseif (y1 < Vmin)
        y1 = Vmin
endif
if (s1 > (Vmax – y1))
        s1 = Vmax – y1
elseif (s1 < (Vmin – y1))
        s1 = Vmin – y1
endif
ds1 = Ki × err
if ( (s1 ≥ (Vmax – y1)) and (ds1 ≥ 0.0) )
        ds1 = 0.0
elseif ( (s1 ≤ (Vmin – y1)) and (ds1 ≤ 0.0) )
        ds1 = 0.0
endif
yout = s1 + y1
```

D. SVS MODEL PARAMETER LISTS

SVSMO1 Dynamic Model Parameters:

The table provided below shows all the parameters of *svsmo1*. Each parameter is explained and a typical range of values provided. Where "N/A" is listed in the typical range of values column, this means that the value is based on specifications, design and tuning and so a typical range is really not applicable to this parameter. The model is per unitized on the SYSTEM MVA BASE. In North America, typically a system MVA base of 100 MVA is used. So for example, the Bmax for a 240 Mvar/-100 Mvar SVC would be 2.4 pu on 100-MVA base.

Parameter	Description	Typical Range of Values	Units
vrefmax[10]	The maximum allowable voltage reference setpoint of the AVR	1.04 to 1.06	pu
vrefmin	The minimum allowable voltage reference setpoint of the AVR	0.99 to 1.01	pu
UVSBmax	Maximum capacitive limit of the SVC during undervoltage strategy	Typically the total shunt capacitance of the fixed filter banks	pu
UV1	Under voltage setpoint 1, below which the SVC output is limited to UVSBmax	N/A	pu
UV2	Under voltage setpoint 2, below which the SVC output is forced to its inductive limit	N/A	pu
UVT	Under voltage trip setpoint, below which the SVC will trip if the voltage stays below this value for UVtm2 seconds.	N/A	pu
OV1	Over voltage setpoint 1, above which the SVC output I forced to its inductive limit; also SVC trips if voltage is above this value for more than OVtm1 seconds.	N/A	pu
OV2	Over voltage setpoint 2, above which the SVC will trip if the voltage stays above this value for OVtm2 seconds.	N/A	pu
UVtm1	Under voltage time 1 (see PLL delay for explanation)	1 to 2 seconds	s
UVtm2	Under voltage trip time (time after which SVC trips when V < UVT)	N/A	s
OVtm1	Over voltage trip time 1 (SVC trips if voltage is above OV1 for this time)	N/A	s
OVtm2	Over voltage trip time 2 (SVC trips if voltage is above OV2 for this time)	N/A	s
mssbus	Bus number in the powerflow where the MSSs are located	N/A	N/A
Mssid1	Id of the first MSS	N/A	N/A
Mssid2	Id of the second MSS	N/A	N/A

[10] vrefmax/vrefmin in GE PSLT® are modeled in the powerflow data card.

Parameter	Description	Typical Range of Values	Units
Mssid3	Id of the third MSS	N/A	N/A
Mssid4	Id of the fourth MSS	N/A	N/A
Mssid5	Id of the fifth MSS	N/A	N/A
Mssid6	Id of the sixth MSS	N/A	N/A
Mssid7	Id of the seventh MSS	N/A	N/A
Mssid8	Id of the eighth MSS	N/A	N/A
flag1	0 – no switching of MSS; 1 – MSS switching enabled	N/A	N/A
flag2	0 – linear slope; 1 – non-linear slope	0	N/A
Xc1	Slope (nominal linear slope; first part of piecewise linear slope)	0.01 to 0.05	pu/pu
Xc2	Slope of second section of piecewise linear slop	N/A	pu/pu
Xc3	Slope of third section of piecewise linear slope	N/A	pu/pu
Vup	Upper voltage break-point of non-linear slope	N/A	pu
Vlow	Lower voltage break point of non-linear slope	N/A	pu
Tc1	Voltage measurement lead time constant	0	s
Tb1	Voltage measurement lag time constant	0.025 – 0.05	s
Tc2	Lead time constant for transient gain reduction	0	s
Tb2	Lag time constant for transient gain reduction	0	s
Kpv	Voltage regulator proportional gain	0	pu/pu/s
Kiv	Voltage regulator integral gain	50 – 500	pu/pu
vemax	Maximum allowable voltage error	N/A (typically set to 999 to ignore)	pu
vemin	Minimum allowable voltage error	N/A (typically set to -999 to ignore)	pu
T2	Firing delay time constant	0.005 – 0.01	s
Bshrt	Short-term maximum capacitive rating of the SVC	N/A	pu
Bmax	Maximum continuous capacitive rating of the SVC	N/A	pu
Bmin	Minimum continuous inductive rating of the SVC	N/A	pu
Tshrt	Short-term rating definite time delay	N/A	s
Kps	Proportional gain of slow-susceptance regulator	0	pu/pu
Kis	Integral gain of slow-susceptance regulator	0.0005 – 0.001	pu/pu/s
Vrmax	Maximum allowed PI controller output of slow-susceptance regulator	0.05 – 0.1	pu
Vrmin	Minimum allowed PI controller output of slow-susceptance regulator	-0.1 – -0.05	pu
Vdbd1	Steady-state voltage deadband; SVC is inactive between Vref+Vdbd1 to Vref-Vdbd1	N/A	pu
Vdbd2	Inner deadband; i.e., when SVC goes outside of Vdbd1, it must come back within the range Vref+Vdbd2 to Vref-Vdbd2 for Tdbd seconds in order for the SVC to be locked again in side Vdbd1.	One fifth to one tenth Vdbd1	pu
Tdbd	Definite time deadband delay	0.1 – 0.5 seconds	s

Parameter	Description	Typical Range of Values	Units
PLLdelay	PLL delay in recovering if voltage remains below UV1 for more than UVtm1 seconds.	0.1	s
Eps	Small delta added to the susceptance bandwidth of the slow-susceptance regulator in order to ensure its limits are not exactly identical to the MSS switching point	0.1	Mvar
Blcs	Large threshold for switching MSS on the capacitive side	N/A	Mvar[11]
Bscs	Small threshold for switching MSS on the capacitive side	N/A	Mvar
Blis	Large threshold for switching MSS on the inductive side	N/A	Mvar
Bsis	Small threshold for switching MSS on the inductive side	N/A	Mvar
Tmssbrk	MSS breaker switching delay (for opening and closing; assume the same for all MSS)	N/A	s
Tdelay1	Definite time delay for larger threshold switching	0.2 – 0.5	s
Tdelay2	Definite time delay for small threshold switching	120 – 300	s
Tout	Discharge time for mechanically switched capacitors	300	s

SVSMO2 Dynamic Model Parameters:

The table provided below shows all the parameters of *svsmo2*. Each parameter is explained and a typical range of values provided. Where "N/A" is listed in the typical range of values column, this means that the value is based on specifications, design and tuning and so a typical range is really not applicable to this parameter. The model is per unitized on the SYSTEM MVA BASE. **NOTE:** *Bmax and Bmin (i.e. the maximum continuous capacitive/inductive rating of the SVC) is determined internally by the model based on the defined number and size of TSC and TSR branches in powerflow.*

Parameter	Description	Typical Range of Values	Units
vrefmax	The maximum allowable voltage reference setpoint of the AVR	1.04 to 1.06	pu
vrefmin	The minimum allowable voltage reference setpoint of the AVR	0.99 to 1.01	pu
UVSBmax	Maximum capacitive limit of the SVC during undervoltage strategy	For a TSC/TSR SVC this will typically be zero (i.e. all TSC/TSRs blocked)	pu
UV1	Under voltage setpoint 1, below which the SVC output is limited to UVSBmax	N/A	pu

[11] The Mvar values here for the MSS switching points really refer to a susceptance. That is, if we set Blcs = 100 Mvar, what we really mean is when the SVC susceptance goes above 1 pu on a 100-MVA base (i.e., the susceptance at which for 1 pu voltage the SVC output would be 100 Mvar) an MSS will be switched.

Parameter	Description	Typical Range of Values	Units
UV2	Under voltage setpoint 2, below which the SVC output is forced to its inductive limit	N/A	pu
UVT	Under voltage trip setpoint, below which the SVC will trip if the voltage stays below this value for UVtm2 seconds.	N/A	pu
OV1	Over voltage setpoint 1, above which the SVC output I forced to its inductive limit; also SVC trips if voltage is above this value for more than OVtm1 seconds.	N/A	pu
OV2	Over voltage setpoint 2, above which the SVC will trip if the voltage stays above this value for OVtm2 seconds.	N/A	pu
UVtm1	Under voltage time 1 (see PLL delay for explanation)	1 to 2 seconds	s
UVtm2	Under voltage trip time (time after which SVC trips when V < UVT)	N/A	s
OVtm1	Over voltage trip time 1 (SVC trips if voltage is above OV1 for this time)	N/A	s
OVtm2	Over voltage trip time 2 (SVC trips if voltage is above OV2 for this time)	N/A	s
mssbus	Bus number in the powerflow where the MSSs are located	N/A	N/A
Mssid1	Id of the first MSS	N/A	N/A
Mssid2	Id of the second MSS	N/A	N/A
Mssid3	Id of the third MSS	N/A	N/A
Mssid4	Id of the fourth MSS	N/A	N/A
Mssid5	Id of the fifth MSS	N/A	N/A
Mssid6	Id of the sixth MSS	N/A	N/A
Mssid7	Id of the seventh MSS	N/A	N/A
Mssid8	Id of the eighth MSS	N/A	N/A
flag1	0 – no switching of MSS; 1 – MSS switching enabled	N/A	N/A
flag2	0 – linear slope; 1 – non-linear slope	0	N/A
Xc1	Slope (nominal linear slope; first part of piecewise linear slope)	0.01 to 0.05	pu/pu
Xc2	Slope of second section of piecewise linear slop	N/A	pu/pu
Xc3	Slope of third section of piecewise linear slope	N/A	pu/pu
Vup	Upper voltage break-point of non-linear slope	N/A	pu
Vlow	Lower voltage break point of non-linear slope	N/A	pu
Tc1	Voltage measurement lead time constant	0	s
Tb1	Voltage measurement lag time constant	0.025 – 0.05	s
Tc2	Lead time constant for transient gain reduction	0	s
Tb2	Lag time constant for transient gain reduction	0	s
Kpv	Voltage regulator proportional gain	0	pu/pu/s
Kiv	Voltage regulator integral gain	50 – 500	pu/pu
vemax	Maximum allowable voltage error	N/A (typically set to 999 to ignore)	pu

Parameter	Description	Typical Range of Values	Units
vemin	Minimum allowable voltage error	N/A (typically set to -999 to ignore)	pu
T2	Firing delay time constant	0.005 – 0.01	s
Bshrt	Short-term maximum capacitive rating of the SVC	N/A	pu
Tshrt	Short-term rating definite time delay	N/A	s
Kps	Proportional gain of slow-susceptance regulator	0	pu/pu
Kis	Integral gain of slow-susceptance regulator	0.0005 – 0.001	pu/pu/s
Vrmax	Maximum allowed PI controller output of slow-susceptance regulator	0.05 – 0.1	pu
Vrmin	Minimum allowed PI controller output of slow-susceptance regulator	-0.1 – -0.05	pu
Vdbd1	Steady-state voltage deadband; SVC is inactive between Vref+Vdbd1 to Vref-Vdbd1	N/A	pu
Vdbd2	Inner deadband; i.e., when SVC goes outside of Vdbd1, it must come back within the range Vref+Vdbd2 to Vref-Vdbd2 for Tdbd seconds in order for the SVC to be locked again in side Vdbd1.	One fifth to one tenth Vdbd1	pu
Tdbd	Definite time deadband delay	0.1 – 0.5 seconds	s
PLLdelay	PLL delay in recovering if voltage remains below UV1 for more than UVtm1 seconds.	0.1	s
Eps	Small delta added to the susceptance bandwidth of the slow-susceptance regulator in order to ensure its limits are not exactly identical to the MSS switching point	0.1	Mvar
Blcs	Large threshold for switching MSS on the capacitive side	N/A	Mvar[12]
Bscs	Small threshold for switching MSS on the capacitive side	N/A	Mvar
Blis	Large threshold for switching MSS on the inductive side	N/A	Mvar
Bsis	Small threshold for switching MSS on the inductive side	N/A	Mvar
Tmssbrk	MSS breaker switching delay (for opening and closing; assume the same for all MSS)	N/A	s
Tdelay1	Definite time delay for larger threshold switching	0.2 – 0.5	s
Tdelay2	Definite time delay for small threshold switching	120 – 300	s
Tout	Discharge time for mechanically switched capacitors	300	s
dbe	Voltage error deadband (see section on svsmo2)	0.01	pu
dbb	Susceptance deadband (see Figure 2-11)	N/A	pu

[12] The Mvar values here for the MSS switching points really refer to a susceptance. That is, if we set Blcs = 100 Mvar, what we really mean is when the SVC susceptance goes above 1 pu on a 100-MVA base (i.e., the susceptance at which for 1 pu voltage the SVC output would be 100 Mvar) an MSS will be switched.

SVSMO3 Dynamic Model Parameters:

The table below is a list of all the parameters of the SVSMO3 model. A few pertinent comments should be made. The MSS bus and shunt ids may be part of the powerflow data structures instead of the dynamics model; this is also true of Vrefmax and Vrefmin. For the typical values please note all values provided are simply for guidance, they do not represent all possible values or appropriate settings for any given installation. The user must take great care to consult with equipment vendors to identify what is appropriate for an actual installation. Where "N/A" is listed in the typical range of values column this indicates that there is no typical range to be provided. This model is per unitized on its own MVA BASE. This was chosen to be the case as opposed to the SVSMO1 and SVSMO2 models because small (10 to 20 MVA) STATCOMs are quite common and in fact much more so than transmission level STATCOMS (the opposite is true for SVCs).

Parameter	Description	Typical Range of Values	Units
MBASE	Model MVA base	N/A	MVA
Vrefmax	The maximum allowable voltage reference setpoint of the AVR	1.02 to 1.05	pu
Vrefmin	The minimum allowable voltage reference setpoint of the AVR	0.98 to 1.01	pu
Xc0	Constant linear droop/slope	0.01 to 0.03	pu/pu
Tc1	Voltage measurement lead time constant	0	s
Tb1	Voltage measurement lag time constant	0.05 – 0.1	s
Kp	Voltage regulator proportional gain	0.0	pu/pu
Ki	Voltage regulator integral gain	20 - 200	pu/pu.s
vemax	Voltage error maximum limit	Typically not used	pu
vemin	Voltage error minimum limit	Typically not used	pu
To	Firing sequence control delay	0.001 – 0.005	s
Imax1	Max. continuous current rating (in pu on model MVA base)	1.00 (i.e., rated value on MVA base)	pu
dbd	Voltage control deadband	0.01 – 0.05	pu
Kdbd	Ratio of outer to inner deadband	5 – 10	N/A
Tdbd	Deadband time	0.10	s
Kpr	Proportional gain for slow-reset control	0.0	pu/pu
Kir	Integral gain for slow-reset control	N/A	pu/pu.s
Idbd	Deadband range for slow-reset current controller	N/A	pu
Vrmax	Maximum limit of slow-reset current controller	0.05 to 0.10	pu
Vrmin	Minimum limit of slow-reset current controller	-0.10 to -0.05	pu

Parameter	Description	Typical Range of Values	Units
Ishrt	Max. short-term current rating as a multiple of continuous rating	1.5 to 3	pu
UV1	Voltage at which the STATCOM limit starts to be reduced linearly	0.50	pu
UV2	Voltage below which the STATCOM is blocked	0.20	pu
OV1	Voltage above which the STATCOM limit linearly changes (up to OV2)	1.10	pu
OV2	Voltage above which the STATCOM blocks its output	1.20	pu
Vtrip	Voltage above which the STATCOM trips after Tdelay2 seconds	1.30	pu
Tdelay1	Short-term rating delay	1.00	s
Tdelay2	Trip time for V > Vtrip	0.08	s
ecap	Enable (ecap=1) or disable (ecap=0) MSS switching	0.0	N/A
Iupr	Threshold for switching MSS on the capacitive side	0.50	pu
Ilwr	Threshold for switching MSS on the inductive side	-0.50	pu
TdelLC	Time delay for switching in a shunt	60.0	s
Tout	Discharge time for mechanically switched capacitors	300.0	s
sdelay	PLLdelay for recovery after blocking	0.02	s
I2t	I2t limit (pu I squared T thermal limit – optional)	0.0	pu.pu.s
Reset	Reset rate for I2t limit	0.0	pu.pu
hyst	Hysteresis for I2t limit	0.0	pu
flag1	= 1 slow reset is on; = 0 slow reset is off.	0.0	N/A
flag2	= 1 non-linear droop is on; = 0 non-linear droop is off	0.0	N/A
Xc1	Non-linear droop slope 1	0.01	pu/pu
Xc2	Non-linear droop slope 2	1.00	pu/pu
Xc3	Non-linear droop slope 3	0.01	pu/pu
V1	Non-linear droop upper voltage	1.025	pu
V2	Non-linear droop lower voltage	0.975	pu
Tc2	Lead time constant	0.0	s
Tb2	Lag time constant	0.0	s
Tmssbrk	MSS breaker switch delay (for opening and closing)	0.0	s
mssbus	Bus number in the powerflow where the MSSs are located	N/A	N/A
Mssid1	Id of the first MSS	N/A	N/A
Mssid2	Id of the second MSS	N/A	N/A

Parameter	Description	Typical Range of Values	Units
Mssid3	Id of the third MSS	N/A	N/A
Mssid4	Id of the fourth MSS	N/A	N/A
Mssid5	Id of the fifth MSS	N/A	N/A
Mssid6	Id of the sixth MSS	N/A	N/A
Mssid7	Id of the seventh MSS	N/A	N/A
Mssid8	Id of the eighth MSS	N/A	N/A